

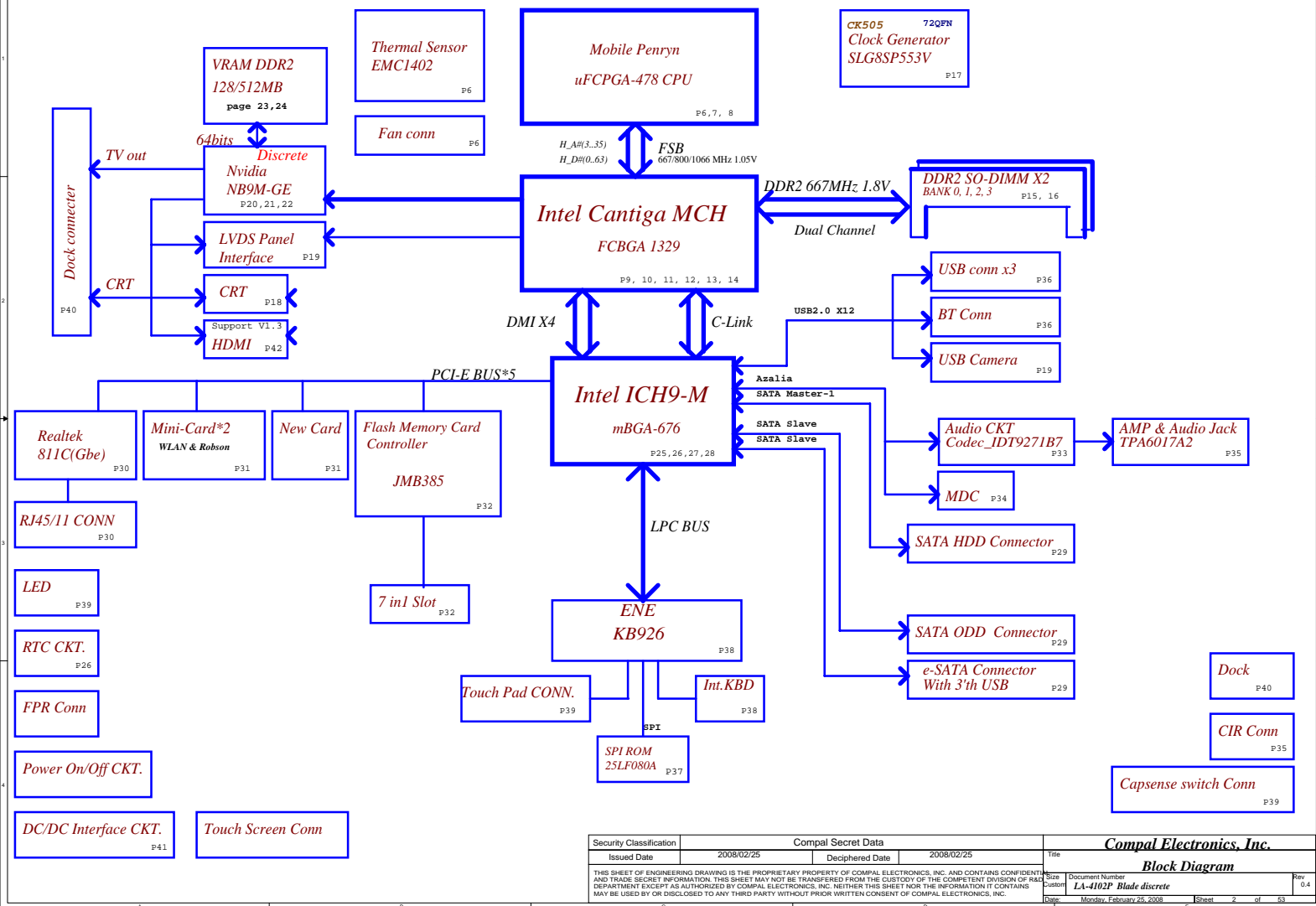
# Compal confidential

## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_PM+ICH9-M core logic

2008-02-25

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Size	Document Number	Rev		
Custom	LA-4102P Blade discrete	0.4		
Date	Monday, February 25, 2008	Sheet	1	of 53



## Voltage Rails

O MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS +NVVDD +PCIE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

## Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build  
DEBUG@ : means just reserve for debug.

## USB assignment:

USB-0 Right side  
USB-1 Right side  
USB-2 Left side(with ESATA)  
USB-3 Dock  
USB-4 Camera  
USB-5 WLAN  
USB-6 Bluetooth  
USB-7 Finger Printer  
USB-8 MiniCard(WWAN/TV)  
USB-9 Express card  
USB-10 X  
USB-11 X

## PCIe assignment:

PCIe-1 TV tuner/WWAN/Robeson  
PCIe-2 X  
PCIe-3 WLAN  
PCIe-4 GLAN (Marvell)  
PCIe-5 Card reader  
PCIe-6 New Card

## SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIF	MINI CARD	Sensor board	NB9M Thermal Sensor	NB9M	G-sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	V	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V	V	X
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V	V	V	X	X	X	V

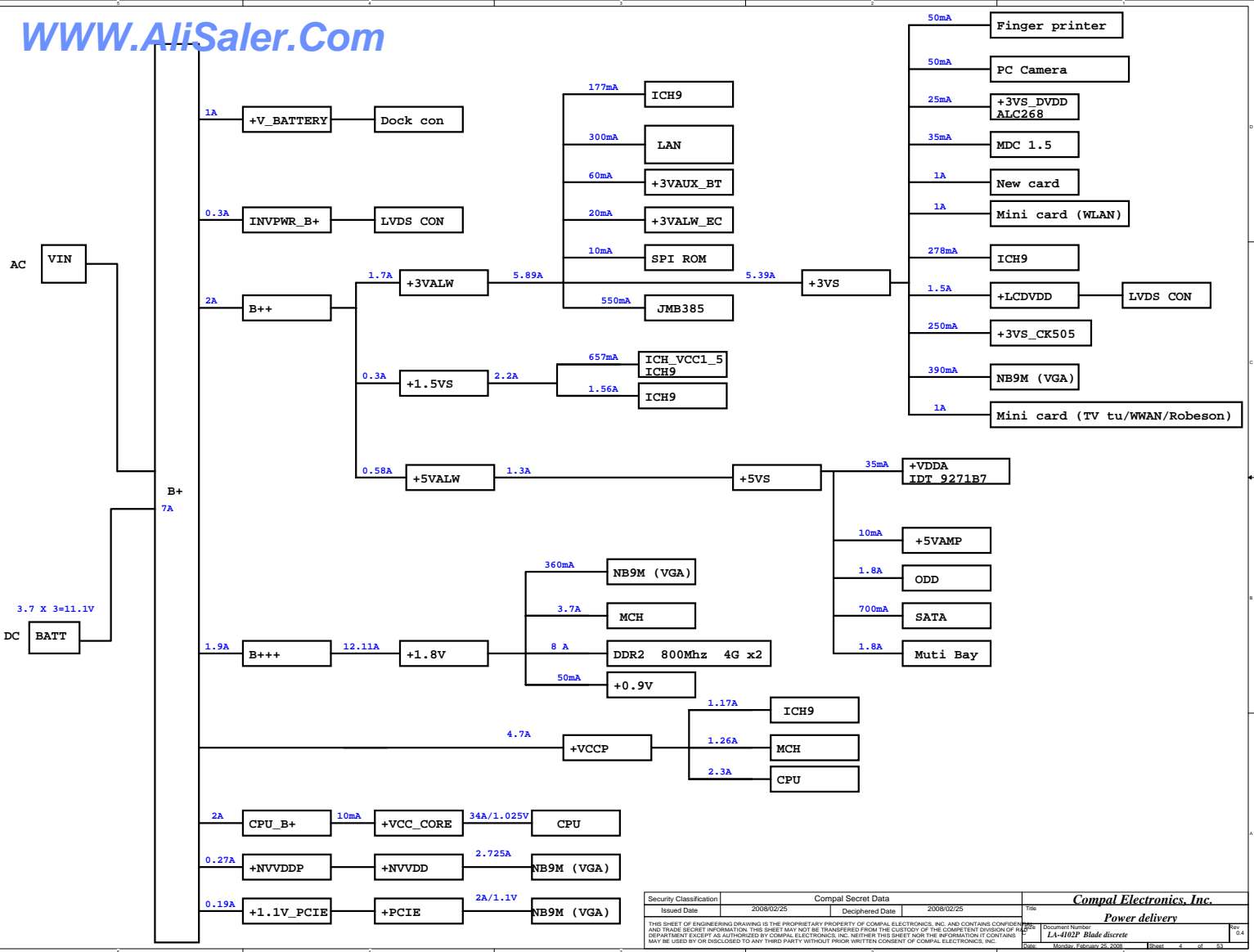
## NB9M SMBUS Control Table

	SOURCE	LVDS	CRT	HDMI
DDC2_DATA DDC2_CLK	NB9M	V	X	X
3VDDCDA 3VDDCCL	NB9M	X	V	X
HDMIDAT_VGA HDMICLK_VGA	NB9M	X	X	V

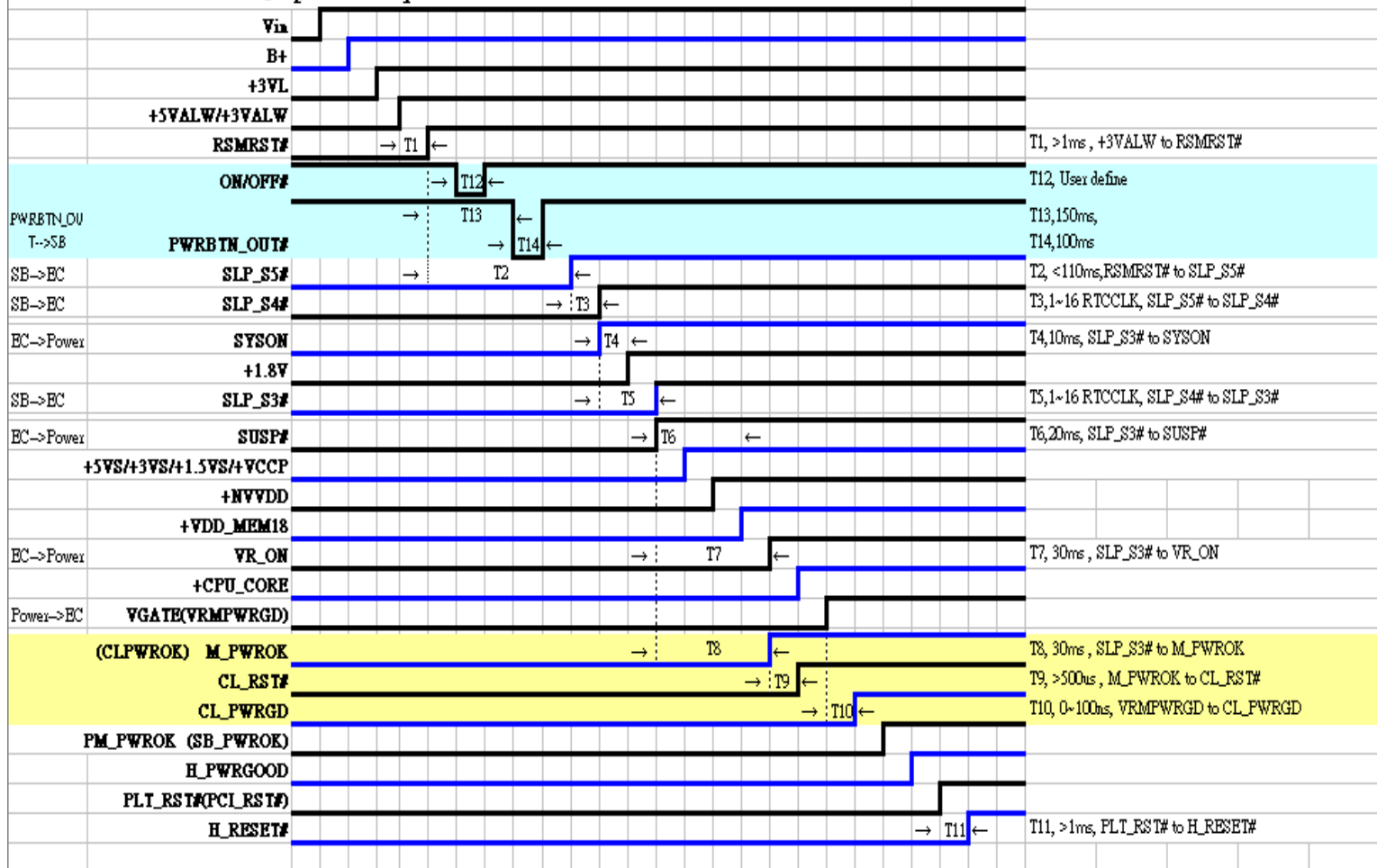
## I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

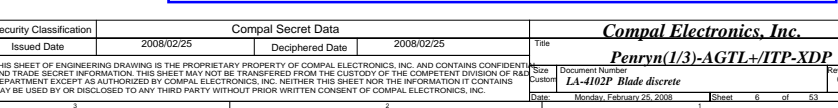
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				Date	Monday, February 25, 2008	Sheet 3 of 63



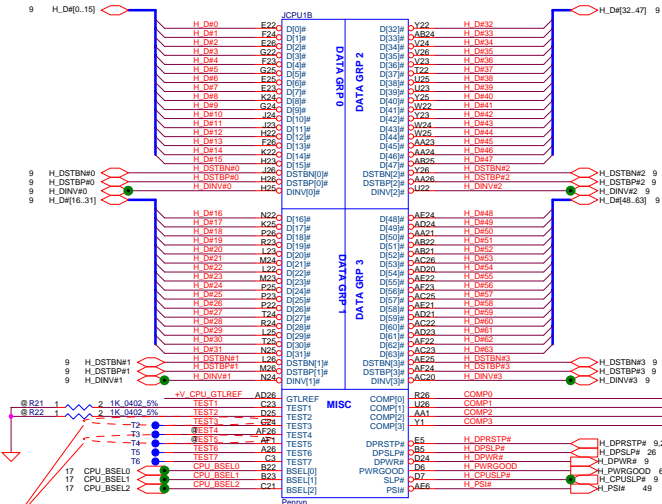
# JAL50 Discrete power sequence AC mode



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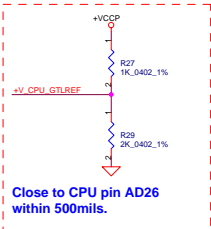
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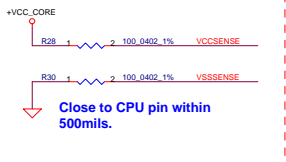
\* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

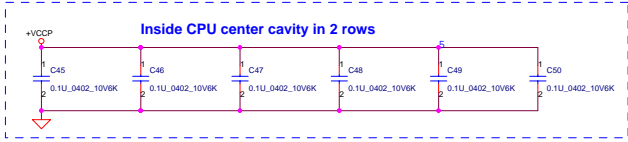
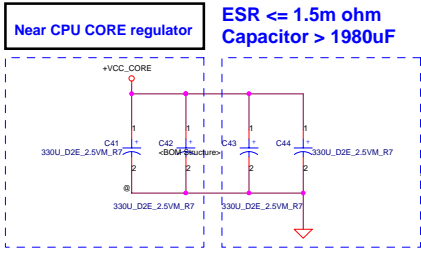
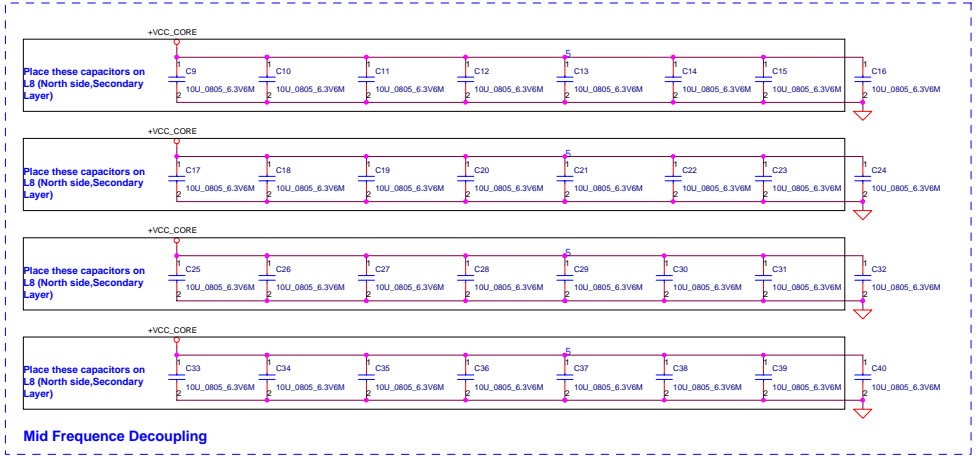


Length match within 25 mils. The trace width/space/other is 20/7/25.



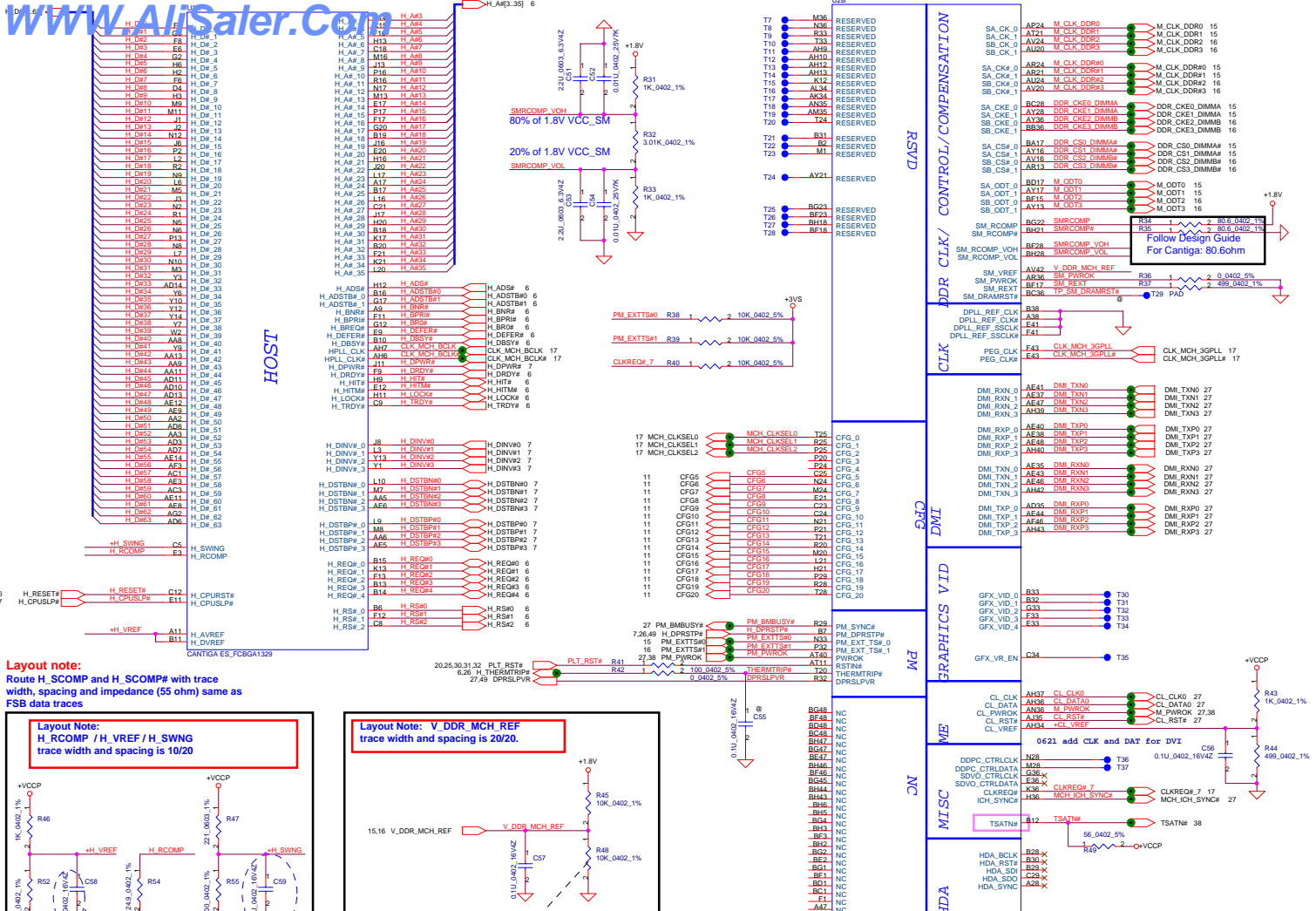
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Size	Document Number	Rev
Customer	LA-4102P Blade discrete	0.4
Date	Monday, February 25, 2008	Sheet 7 of 53

ICPUID		
AA	VSS[001]	P6
AA	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
BB	VSS[009]	T26
BB	VSS[010]	T23
B11	VSS[011]	T2
B13	VSS[012]	T3
B16	VSS[013]	U8
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	U2
CA	VSS[017]	V2
CA	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W2
C19	VSS[022]	W23
C2	VSS[023]	Y3
C22	VSS[024]	Y26
CA5	VSS[025]	Y2
D11	VSS[026]	Y21
D4	VSS[027]	Y24
DA	VSS[028]	Y2
D13	VSS[029]	AA5
D16	VSS[030]	AA8
D19	VSS[031]	AA11
D23	VSS[032]	AA14
D26	VSS[033]	AA15
EA	VSS[034]	AA19
EA	VSS[035]	AA2
EA	VSS[036]	AA25
E11	VSS[037]	AB1
E14	VSS[038]	AB4
E16	VSS[039]	AB8
E19	VSS[040]	AB11
E21	VSS[041]	AB12
E24	VSS[042]	AB15
F2	VSS[043]	AB19
FA	VSS[044]	AB23
FA	VSS[045]	AB26
F11	VSS[046]	AC1
F13	VSS[047]	AC6
F16	VSS[048]	AC11
F19	VSS[049]	AC14
F22	VSS[050]	AC19
F25	VSS[051]	AC24
G1	VSS[052]	AD2
G23	VSS[053]	AD5
G26	VSS[054]	AD8
H3	VSS[055]	AD11
H6	VSS[056]	AD14
H21	VSS[057]	AD19
H24	VSS[058]	AD23
J2	VSS[059]	AD26
J5	VSS[060]	AE1
J22	VSS[061]	AE4
J25	VSS[062]	AE8
K1	VSS[063]	AE11
K4	VSS[064]	AE14
K23	VSS[065]	AE19
K26	VSS[066]	AE23
L3	VSS[067]	AE26
L6	VSS[068]	AF1
L21	VSS[069]	AF4
L24	VSS[070]	AF8
M2	VSS[071]	AF11
M5	VSS[072]	AF14
M22	VSS[073]	AF19
M25	VSS[074]	AF23
N1	VSS[075]	AF26
N4	VSS[076]	AG1
N23	VSS[077]	AG4
N26	VSS[078]	AG8
PA	VSS[079]	AG11
PA	VSS[080]	AG14
PA	VSS[081]	AG19
PA	VSS[082]	AG23
PA	VSS[083]	AG26
PA	VSS[084]	AG29
PA	VSS[085]	AG32
PA	VSS[086]	AG35
PA	VSS[087]	AG38
PA	VSS[088]	AG41
PA	VSS[089]	AG44
PA	VSS[090]	AG47
PA	VSS[091]	AG50
PA	VSS[092]	AG53
PA	VSS[093]	AG56
PA	VSS[094]	AG59
PA	VSS[095]	AG62
PA	VSS[096]	AG65
PA	VSS[097]	AG68
PA	VSS[098]	AG71
PA	VSS[099]	AG74
PA	VSS[100]	AG77
PA	VSS[101]	AG80
PA	VSS[102]	AG83
PA	VSS[103]	AG86
PA	VSS[104]	AG89
PA	VSS[105]	AG92
PA	VSS[106]	AG95
PA	VSS[107]	AG98
PA	VSS[108]	AG101
PA	VSS[109]	AG104
PA	VSS[110]	AG107
PA	VSS[111]	AG110
PA	VSS[112]	AG113
PA	VSS[113]	AG116
PA	VSS[114]	AG119
PA	VSS[115]	AG122
PA	VSS[116]	AG125
PA	VSS[117]	AG128
PA	VSS[118]	AG131
PA	VSS[119]	AG134
PA	VSS[120]	AG137
PA	VSS[121]	AG140
PA	VSS[122]	AG143
PA	VSS[123]	AG146
PA	VSS[124]	AG149
PA	VSS[125]	AG152
PA	VSS[126]	AG155
PA	VSS[127]	AG158
PA	VSS[128]	AG161
PA	VSS[129]	AG164
PA	VSS[130]	AG167
PA	VSS[131]	AG170
PA	VSS[132]	AG173
PA	VSS[133]	AG176
PA	VSS[134]	AG179
PA	VSS[135]	AG182
PA	VSS[136]	AG185
PA	VSS[137]	AG188
PA	VSS[138]	AG191
PA	VSS[139]	AG194
PA	VSS[140]	AG197
PA	VSS[141]	AG200
PA	VSS[142]	AG203
PA	VSS[143]	AG206
PA	VSS[144]	AG209
PA	VSS[145]	AG212
PA	VSS[146]	AG215
PA	VSS[147]	AG218
PA	VSS[148]	AG221
PA	VSS[149]	AG224
PA	VSS[150]	AG227
PA	VSS[151]	AG230
PA	VSS[152]	AG233
PA	VSS[153]	AG236
PA	VSS[154]	AG239
PA	VSS[155]	AG242
PA	VSS[156]	AG245
PA	VSS[157]	AG248
PA	VSS[158]	AG251
PA	VSS[159]	AG254
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PA	VSS[162]	AG263
PA	VSS[163]	AG266

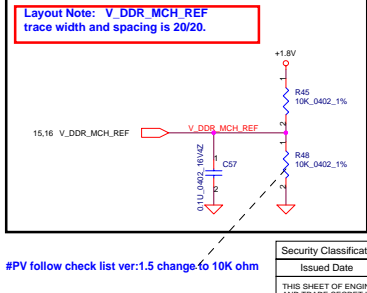
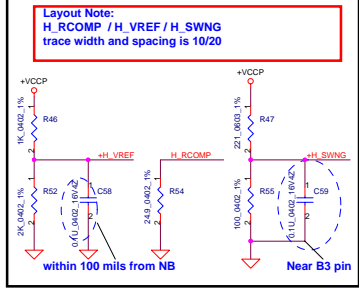


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				Sheet	8 of 53



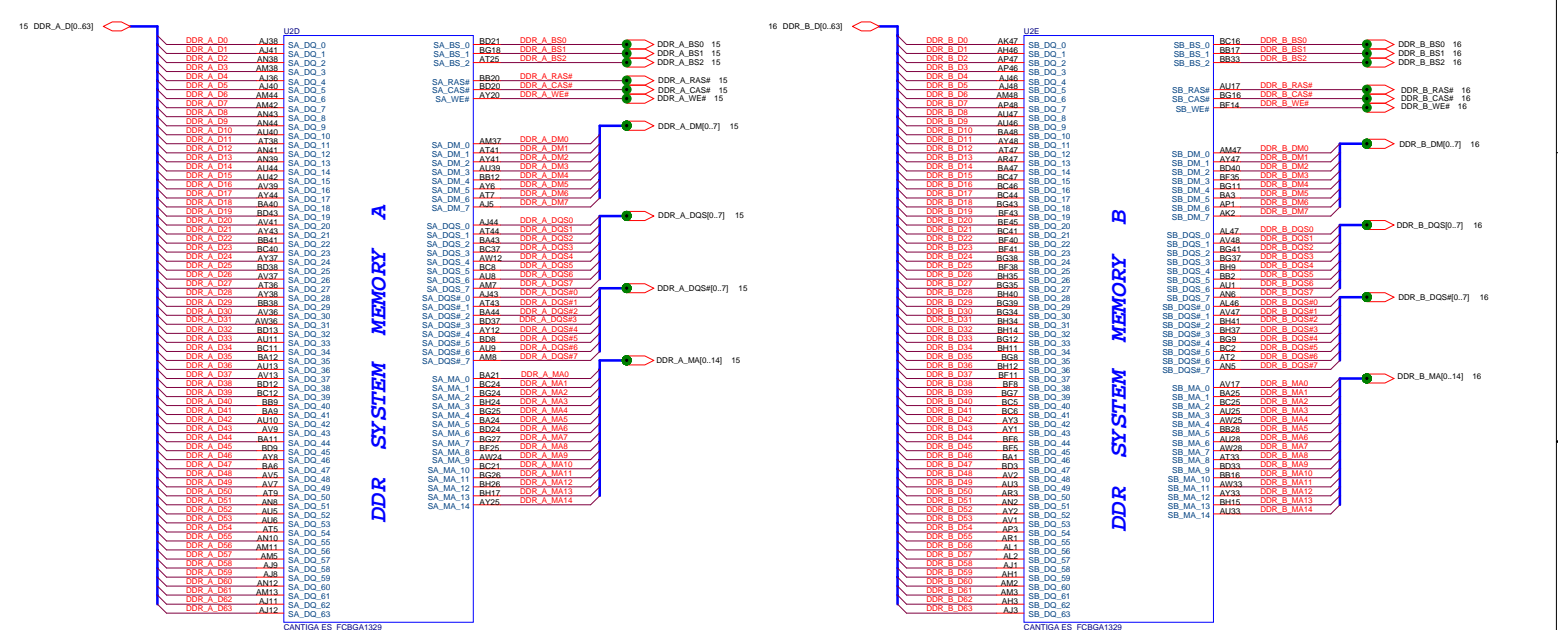


**Layout note:**  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

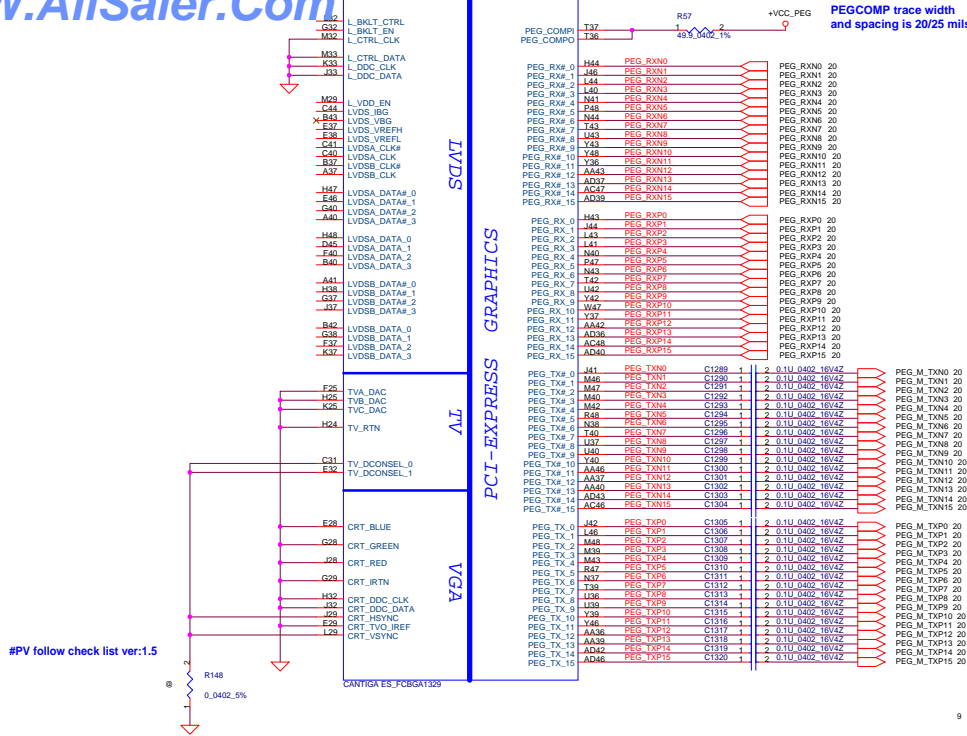


#PV follow check list ver:1.5 change to 10K ohm

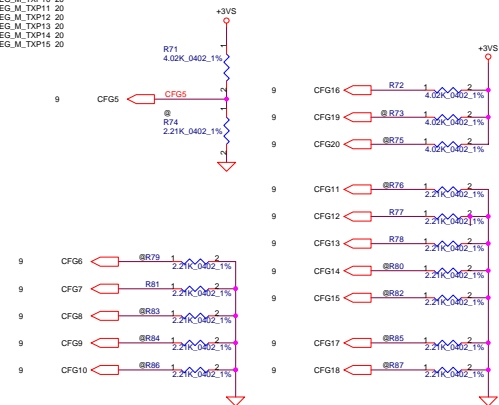
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Date		Sheet	
Monday, February 25, 2008		9 of 53	



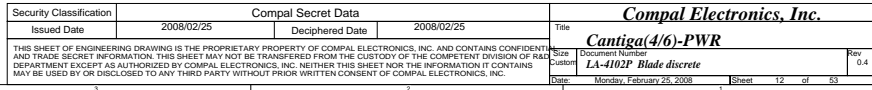
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				Custom
				Date
				Sheet
				of
				53



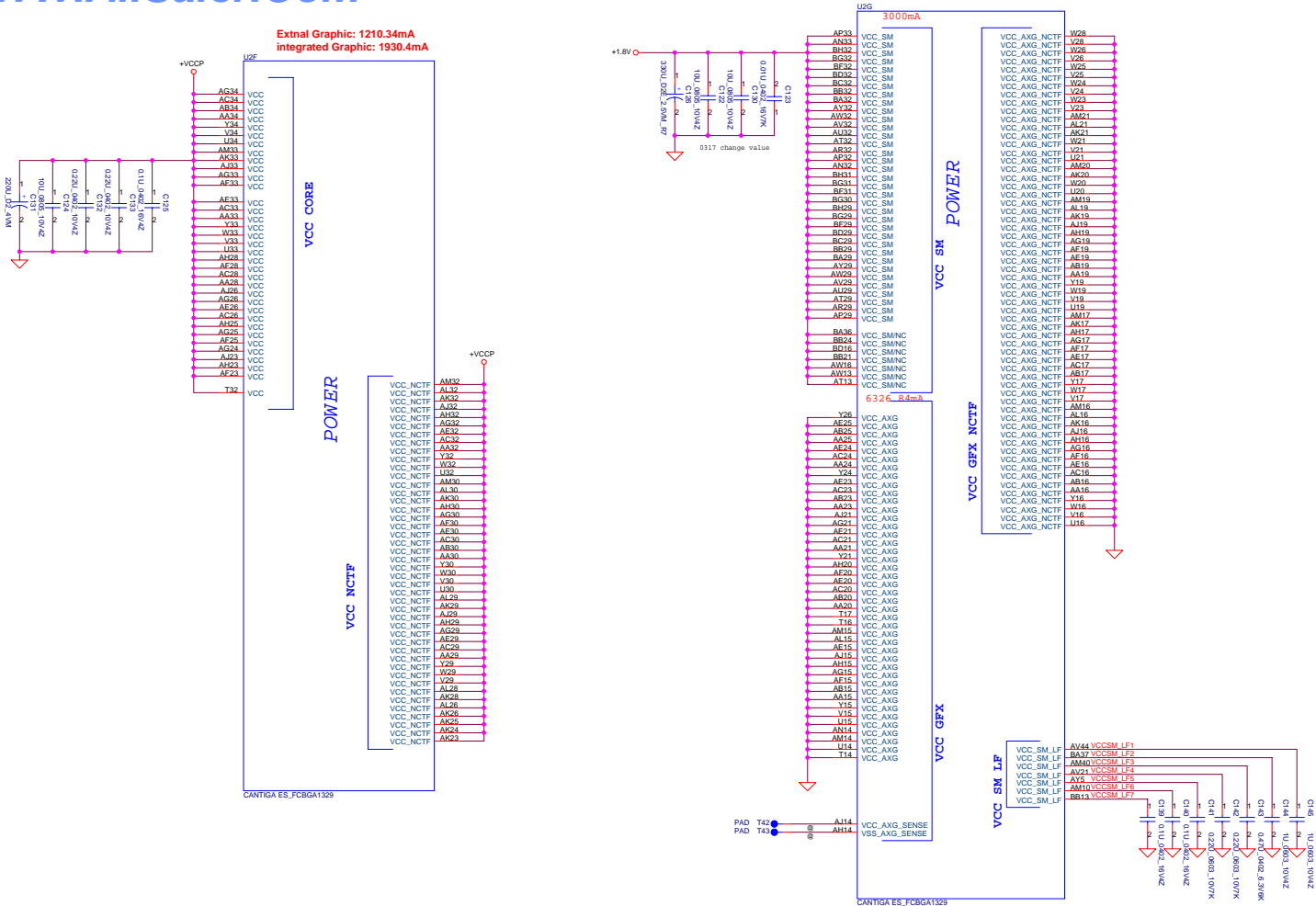
CFG2[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG4[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (T)LSchiper suite with no confidentiality 1 = (T)LSchiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15>0-, 14>-1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG13[12:10] (XAI/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG15[14:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG18[17:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = Both PCIe are operating simu.



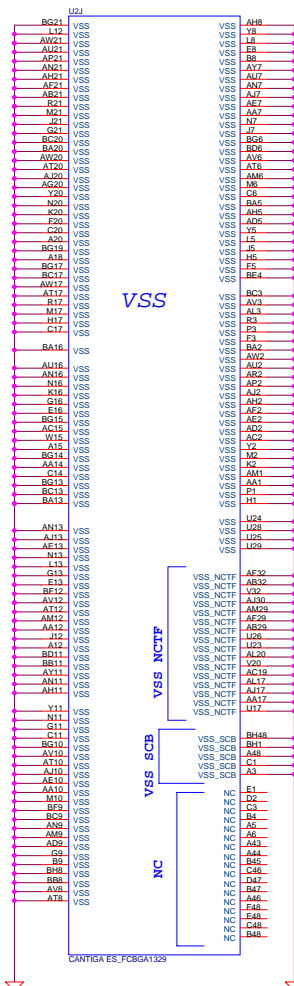
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Date	Issued Date <b>Monday, 24, 2008</b>			Sheet	Rev <b>0.4</b>	
				11	of 53	



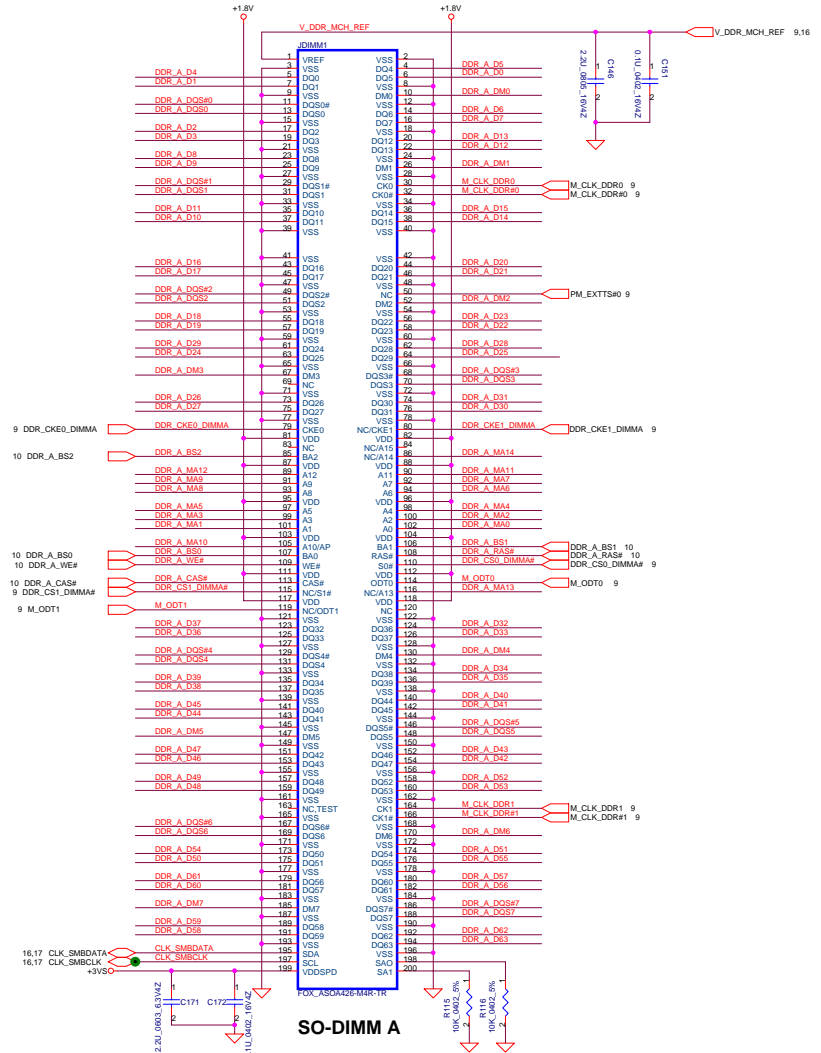
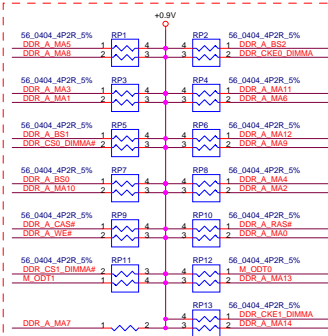
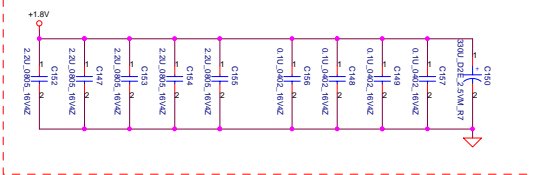
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Integrated Graphic: 1930.4mA



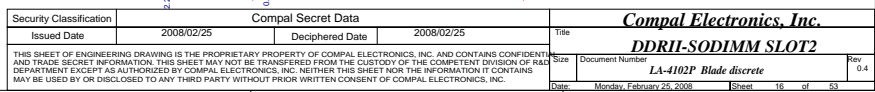
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								Date		Monday, February 25, 2008		Sheet 13 of 53	



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			Date <b>Monday, February 25, 2008</b>	
			Sheet <b>14</b>	of <b>53</b>

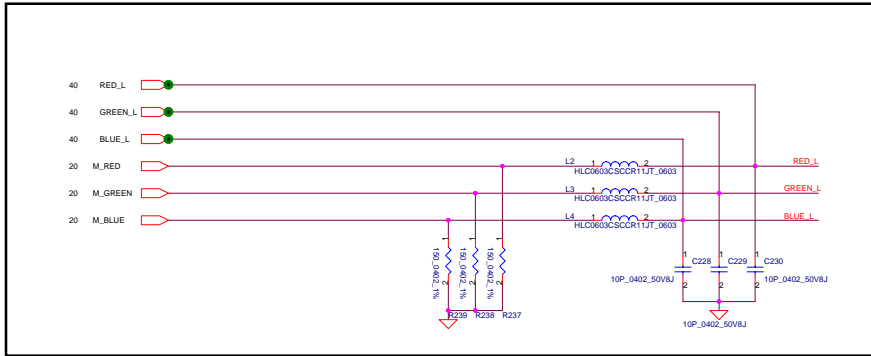
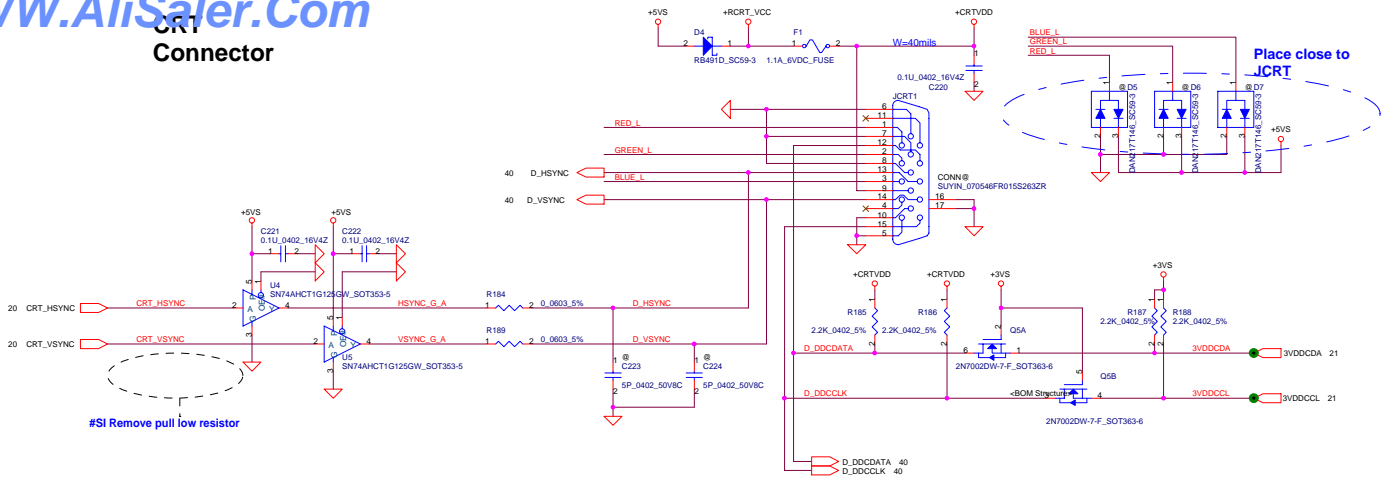


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Date	LA-4102P Blade disclose			Sheet	15	of 53

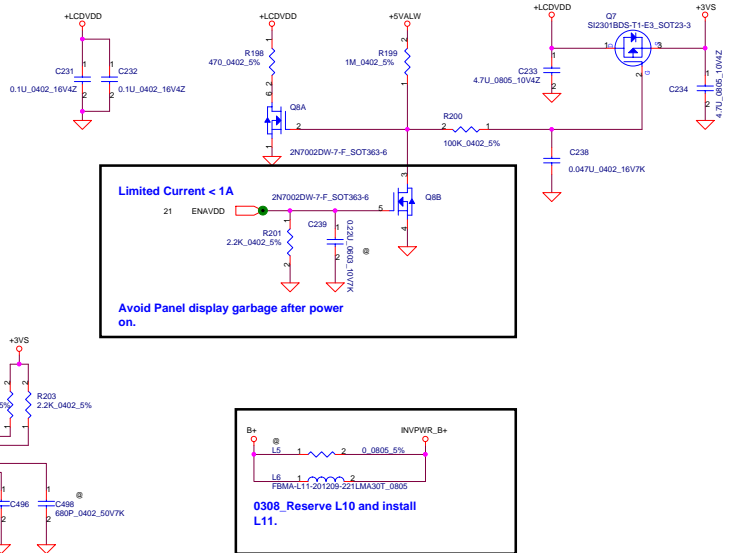






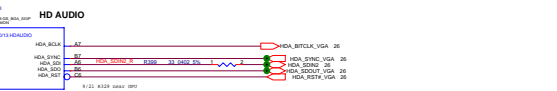
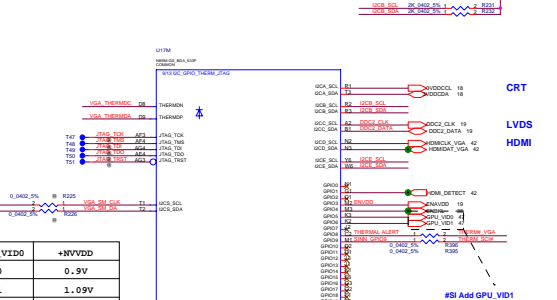
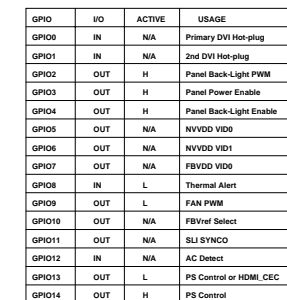
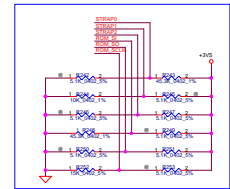


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				0.4
				Date
				Monday, February 25, 2008
				Sheet
				18 of 53



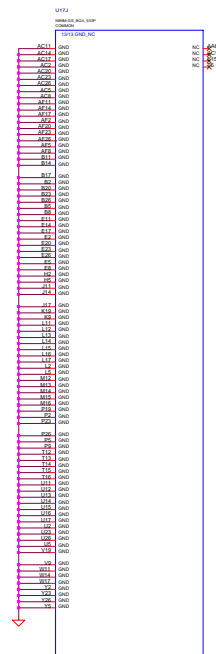
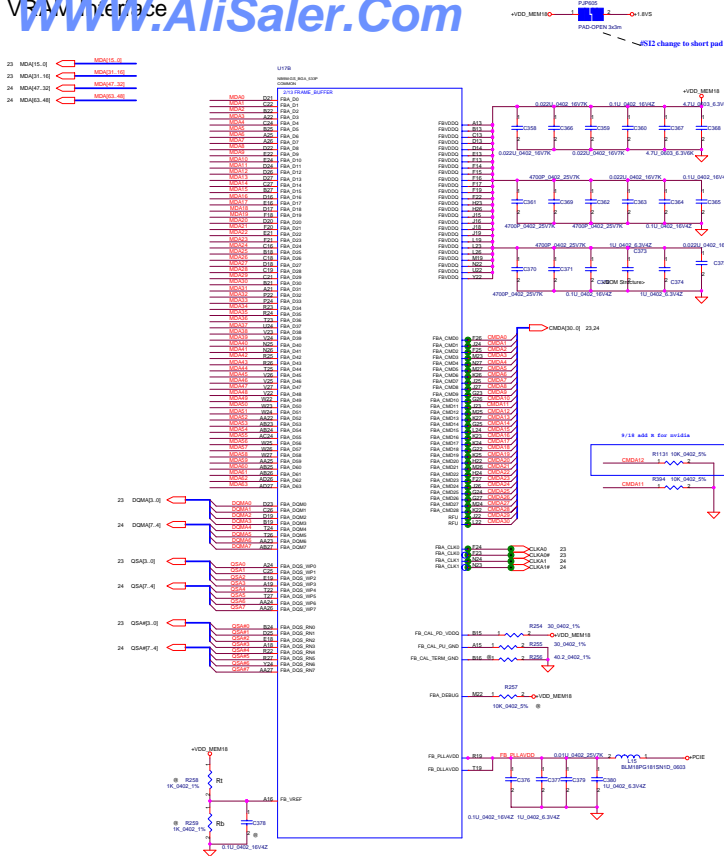
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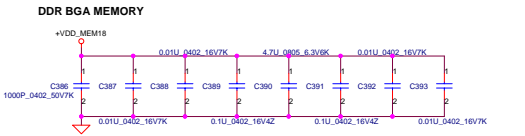
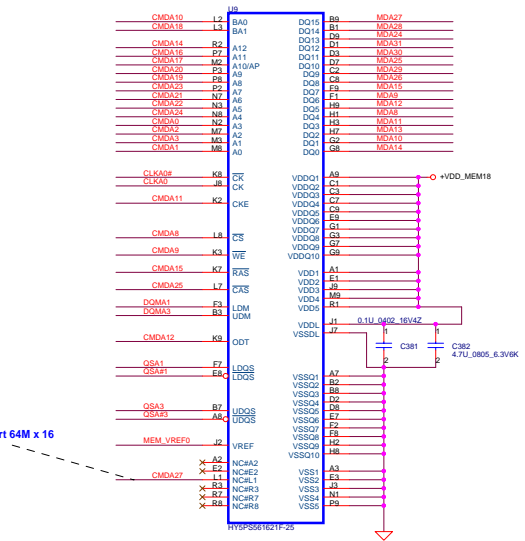
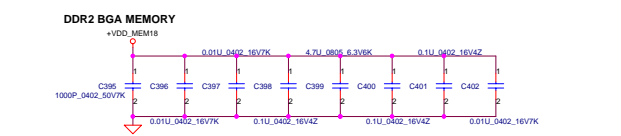
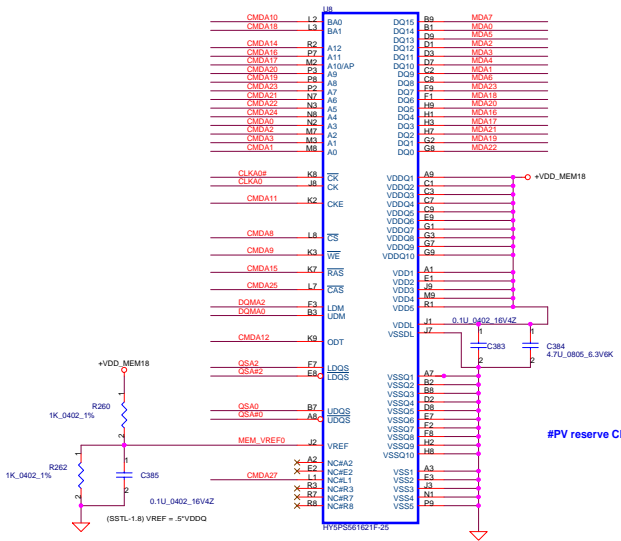
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Sheet	1	Sheet	1	0.4
Page	1	Page	1	0.4

32Mx16 DDR2 400MHz \*4==>256MB  
64Mx16 DDR2 400MHz\*4==>512MB

22.24 QSA[7..0] QSA[7..0]  
22.24 QSA[7..0] QSA[7..0]  
22.24 QMA[7..0] QMA[7..0]  
22.24 MDA[3..0] MDA[3..0]  
22.24 CMA[30..0] CMA[30..0]

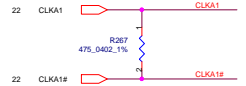
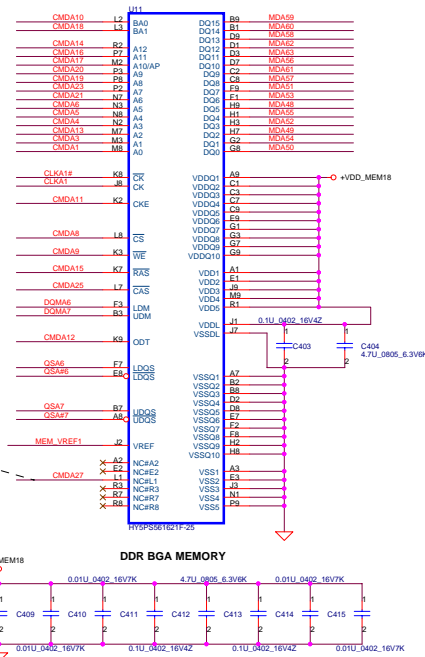
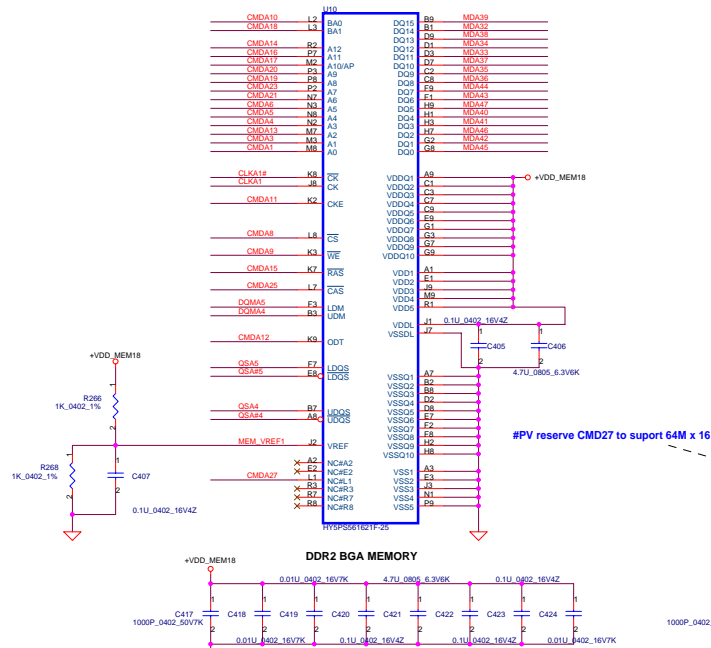


Address	DATA	Bus
CMD0	A3	32..63
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

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		Date	Monday, February 25, 2008
		Sheet	7 of 16

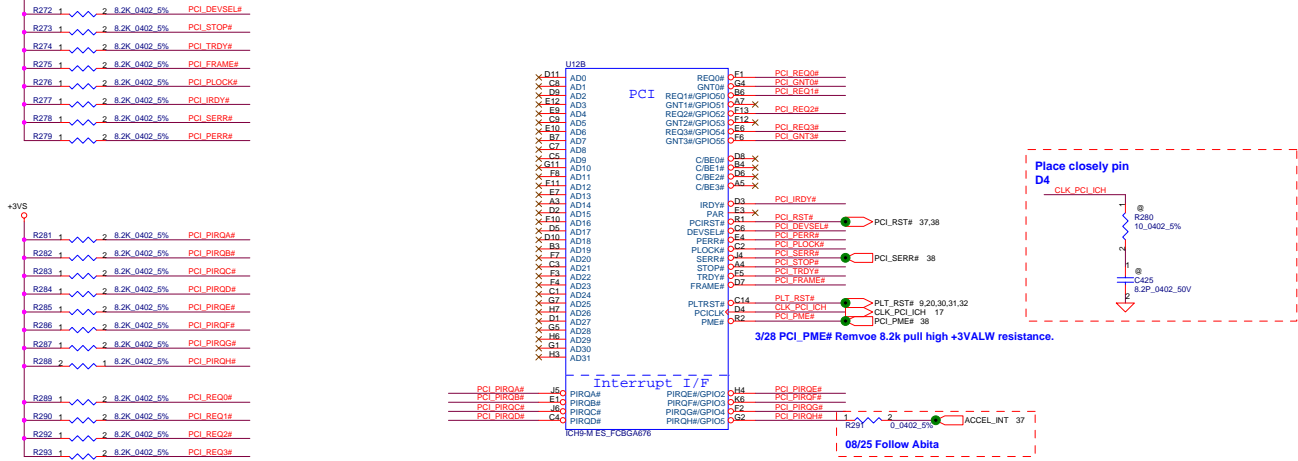
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22.23 CQMA[30..0] <--> CQMA[30..0]  
22.23 QSA[7..0] <--> QSA[7..0]  
22.23 QSA[7..0] <--> QSA[7..0]  
22.23 MDV[63..0] <--> MDV[63..0]

Address	DATA	Bus
CMD0	A3	32..63
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



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		CHANNEL A EXT. 256M 2		Monday, February 25, 2008
		Sheet 8 of 16		





A16 swap override Strap

PCI\_GNT3#

Low= A16 swap override Enble  
High= Default \*

PCI\_GNT3#

1

2

1K\_0402\_5%

Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

27 SPI\_CS1#\_R

SPI\_CS1#\_R

1

2

1K\_0402\_5%

PCI\_GNT0#

1

2

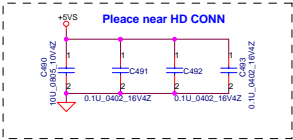
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				LA-4102P	Blade discrete
				Date	Monday, February 25, 2008
				Sheet	26 of 53

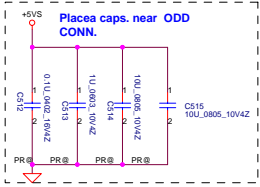
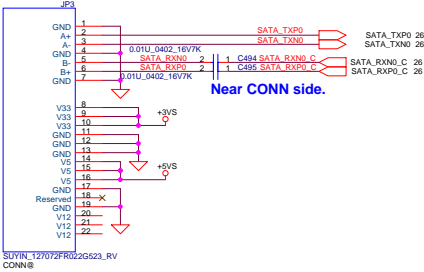




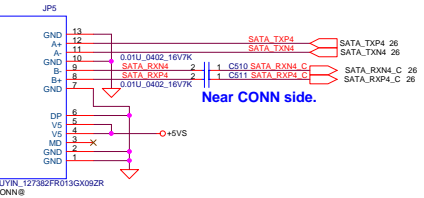




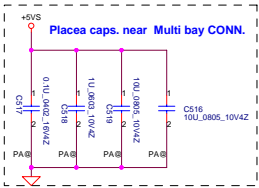
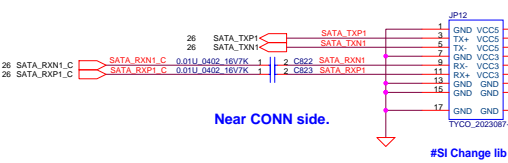
HDD Connector



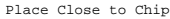
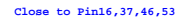
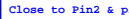
CD-ROM Connector



Multi Bay Connector

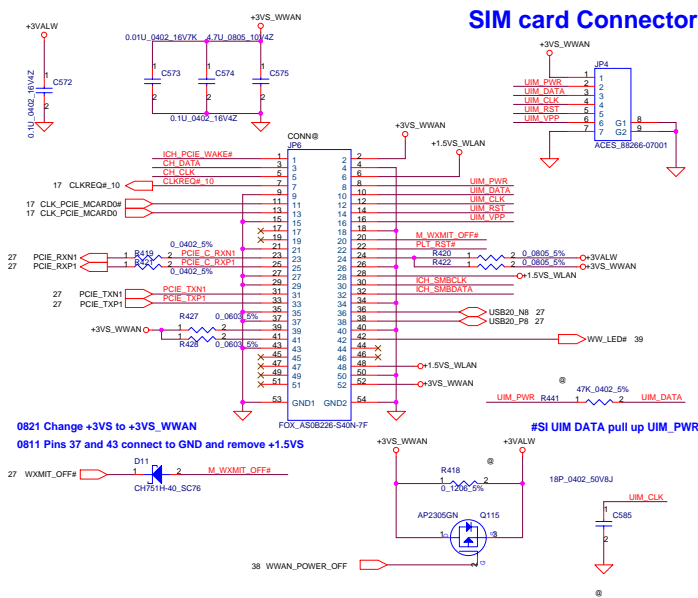


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				LA-4102P Blade discrete
				Rev
				0.4
				Date
				Monday, February 25, 2008
				Sheet
				28 of 53

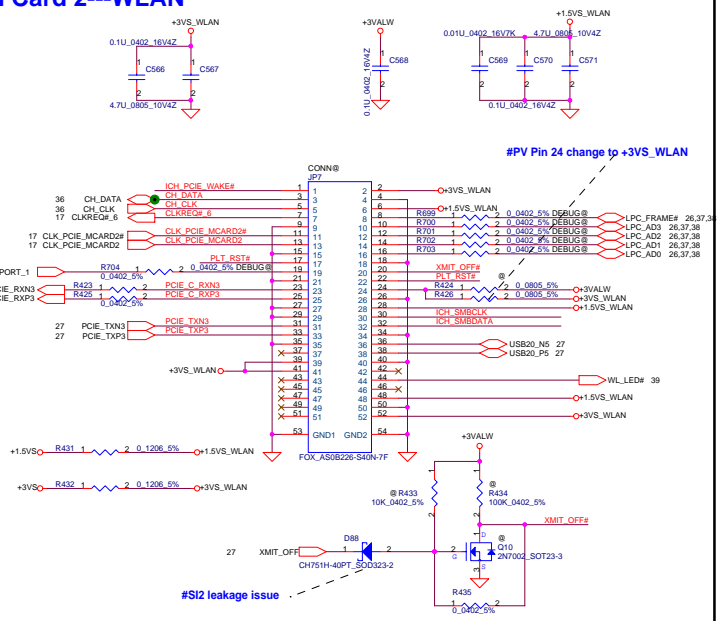


#### Security Classification

## SIM card Connector

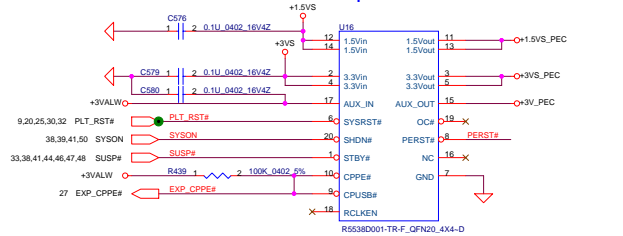


## Mini Card 2---WLAN



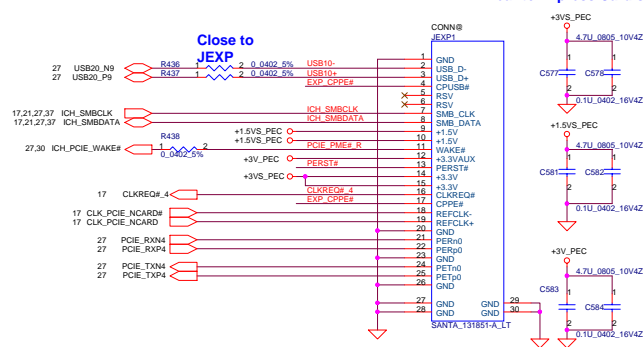
## New Card

### Express Card Power Switch

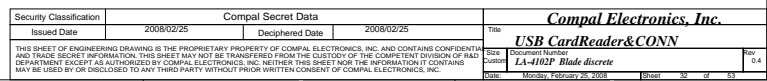


internal pull high to 3.3Vaux-in  
EC need setting at Hi-Z & output Low

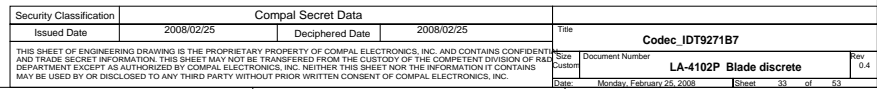
**Near to Express Card slot.**

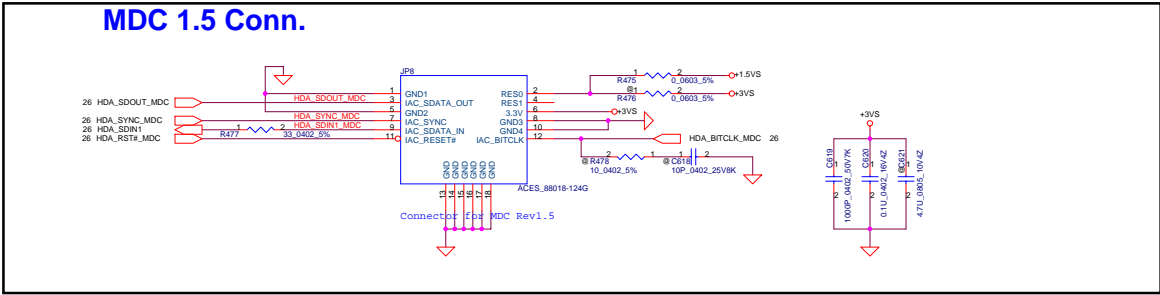


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Date	Monday, February 25, 2008		Sheet	31 of 53

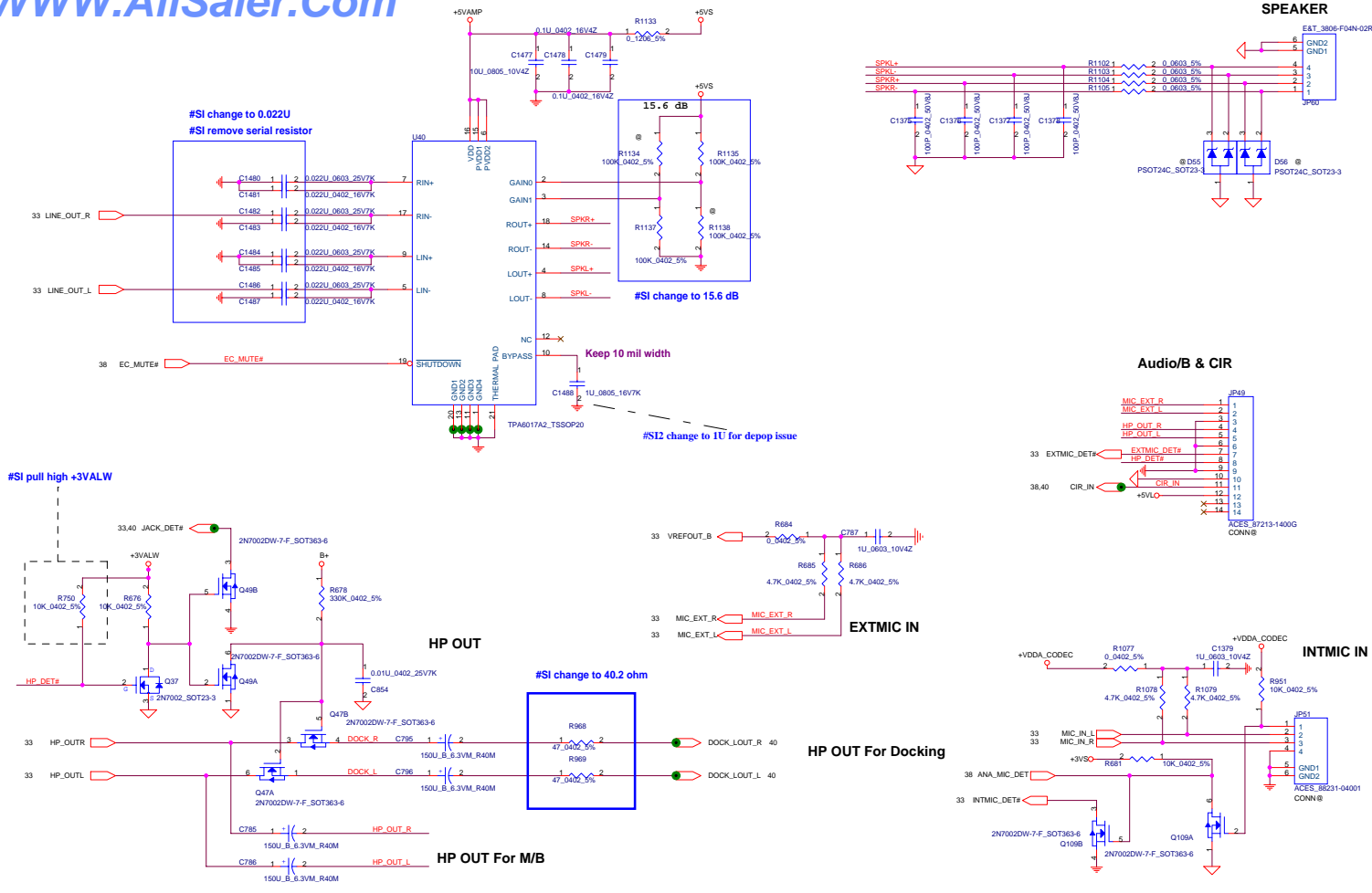






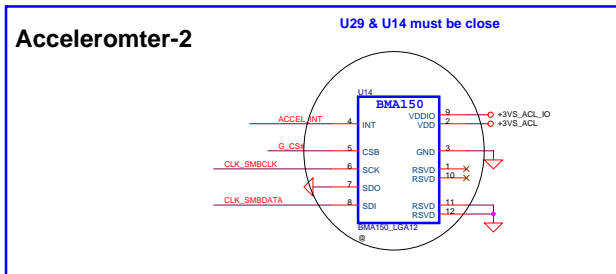
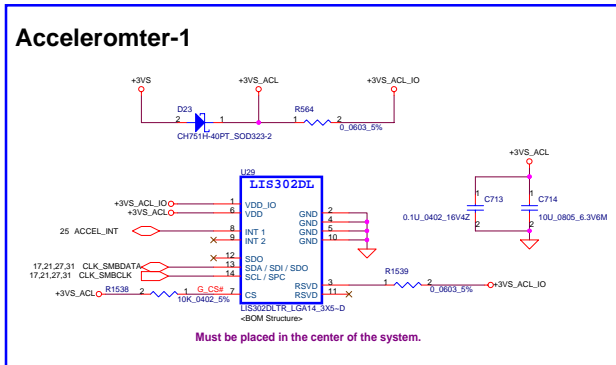
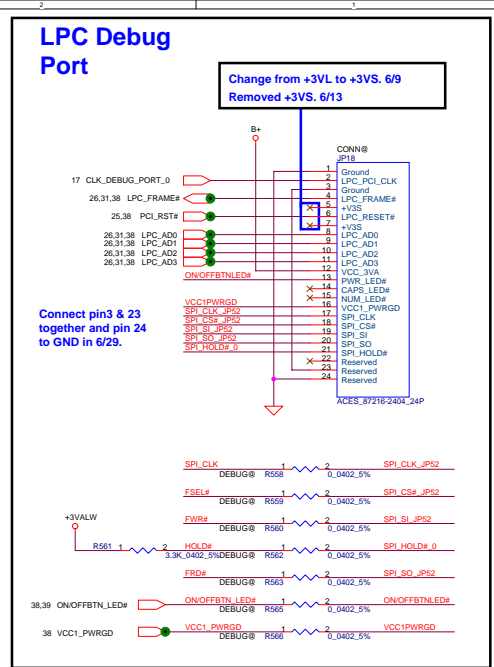
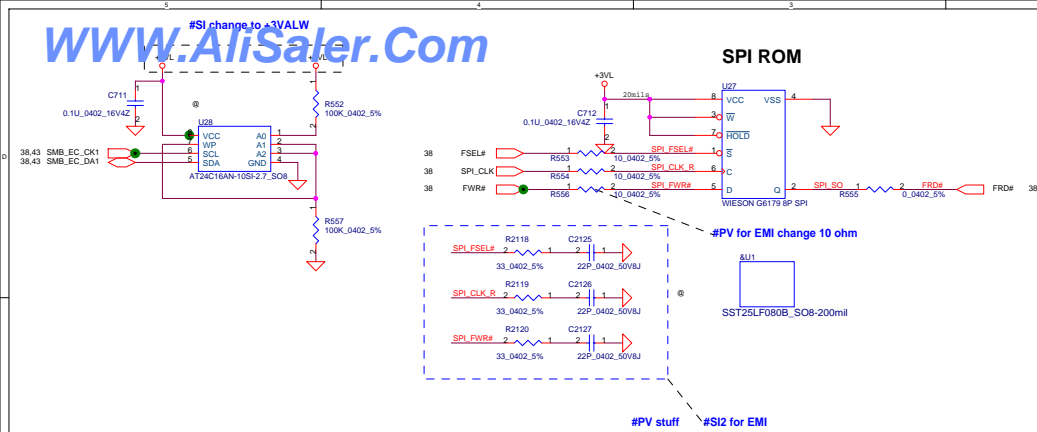


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						LA-4102P Blade discrete	
		Date		Monday, February 25, 2008	Sheet 34 of 53		
				Rev	0.4		

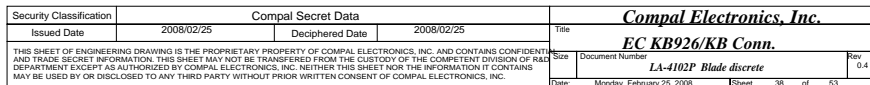


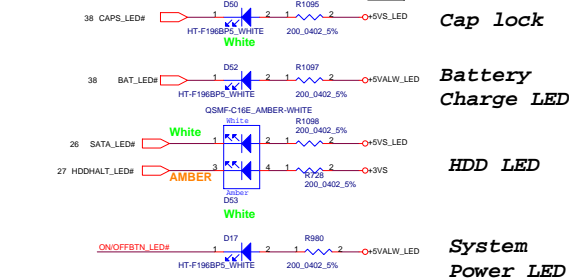
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				Date	Monday, February 25, 2008
				Sheet	35 of 53



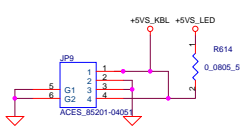


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				Sheet	37 of 53
				Rev	0.4

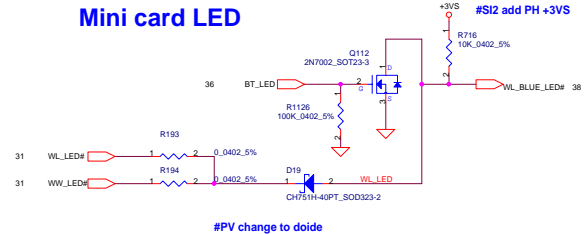




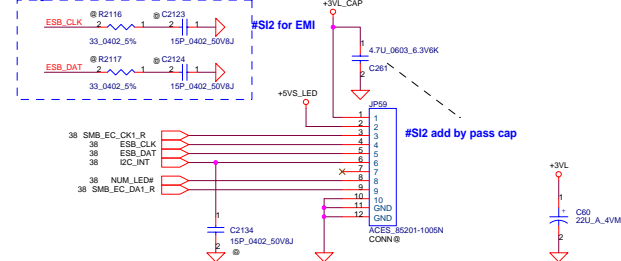
# Keyboard backlight Conn



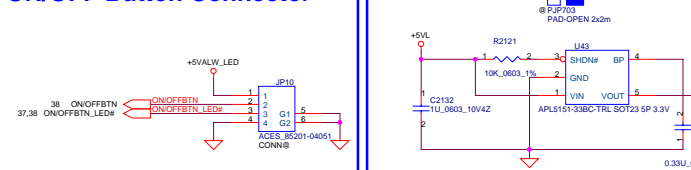
# Mini card LED



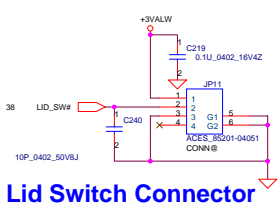
# Capacitor Sensor Conn



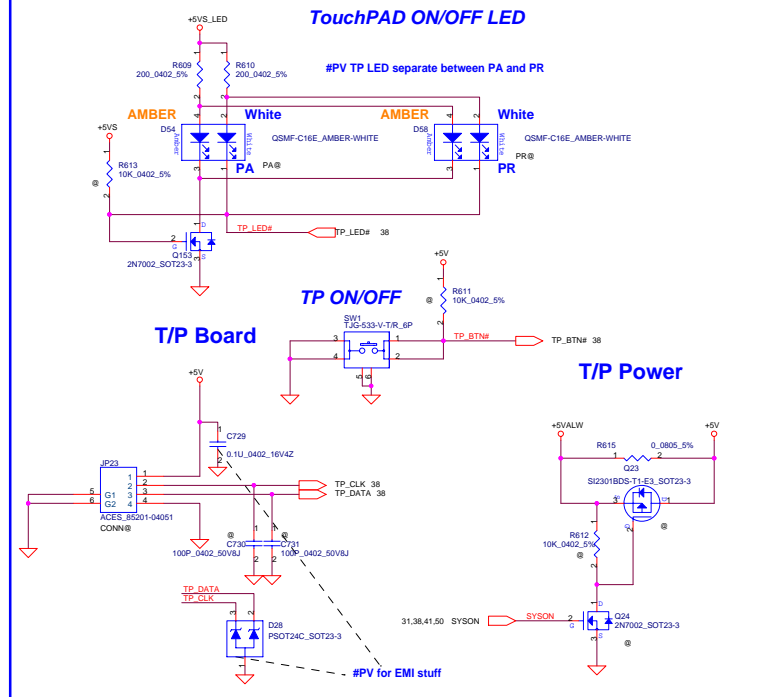
# ON/OFF Button Connector



# Lid Switch Connector



# TouchPAD ON/OFF LED

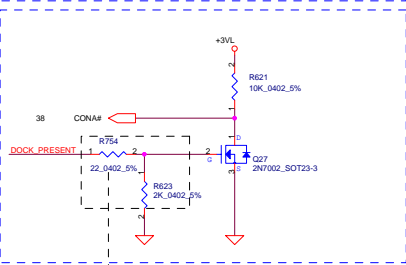
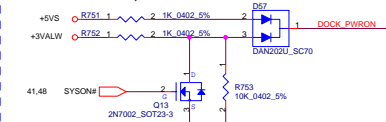


Security Classification	Compal Secret Data		Title	
Issued Date	2008/02/25	Deciphered Date	2008/02/25	LED, TP,KBL,Cab sensor boar
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Date	Monday, February 25, 2008	Sheet	38	of 53

# Atlas/ Saturn Dock

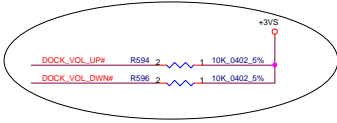
## DOCK\_PWR\_ON Spec

0V = Notebook S4/S5, Dock off  
2.5V = Notebook S3, Dock on  
4V = Notebook S0, Dock on



#SI2 change to 22 ohm

#SI2 Add pull up



18 GREEN\_L  
18 RED\_L  
18 BLUE\_L  
18 D\_D0CDATA  
18 D\_HS1NC  
18 D\_HS2NC  
27 USB20\_P3  
30 R445\_MID3+  
30 R445\_MID3-  
30 R445\_MID2+  
30 R445\_MID2-  
30 R445\_MID1+  
30 R445\_MID1-  
30 R445\_MID0+  
30 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
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20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

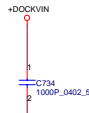
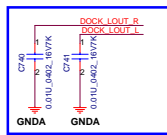
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40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

40 GREEN  
40 RED  
40 BLUE  
40 D\_D0CDATA  
40 D\_HS1NC  
40 D\_HS2NC  
24 USB20\_P3  
20 R445\_MID3+  
20 R445\_MID3-  
20 R445\_MID2+  
20 R445\_MID2-  
20 R445\_MID1+  
20 R445\_MID1-  
20 R445\_MID0+  
20 R445\_MID0-

need change to reverse type connector

11/17 update



#SI2 change ping 31,39,22 connect to GND

#PV reserve resistor

#SI connect to EC

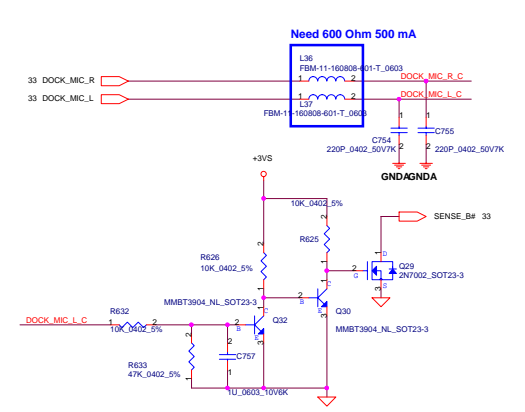
#SI connect to GND

#SI2 add a cap

#SI2 add a cap

#SI2 add a cap

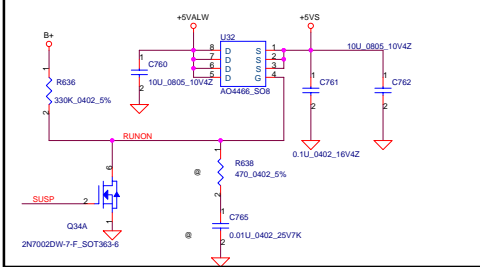
## MIC\_Dock



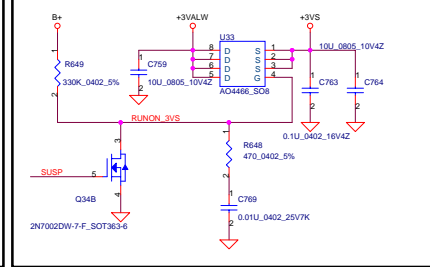
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Issued Date	2008/02/25	Deciphered Date	2008/02/25	Title
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				Rev 0.4
				LA-4102P Blade discrete
				Date: Monday, February 25, 2008
				Sheet 40 of 53



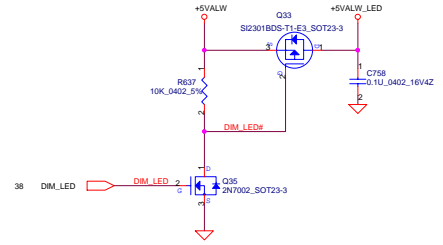
### +5VALW to +5VS Transfer



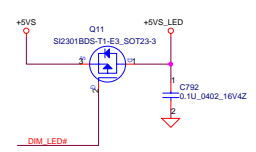
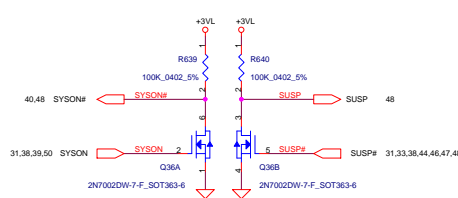
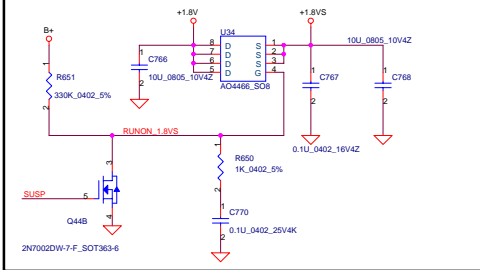
### +3VALW to +3VS Transfer



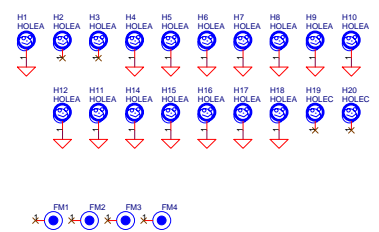
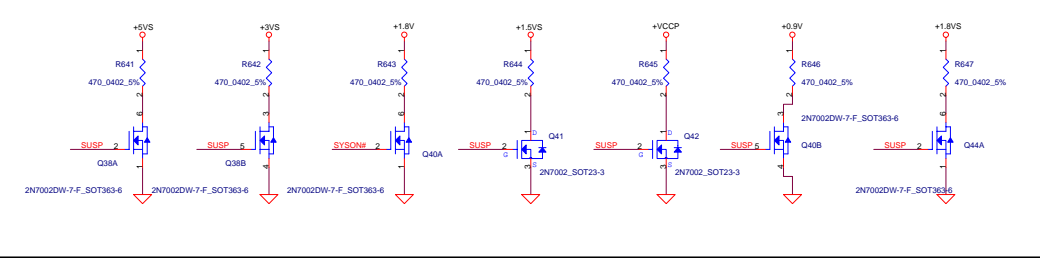
### DIM LED



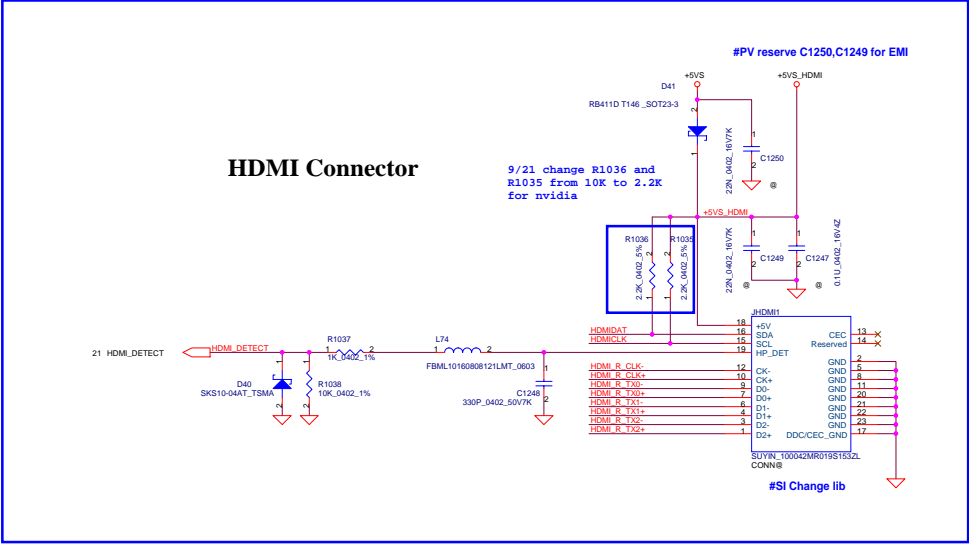
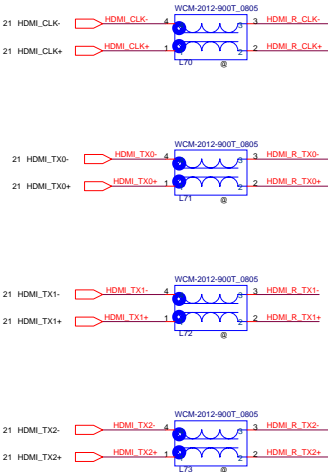
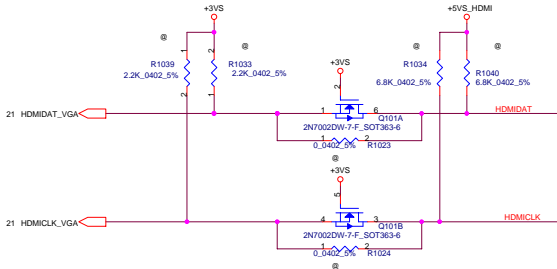
### +1.8V to +1.8VS Transfer



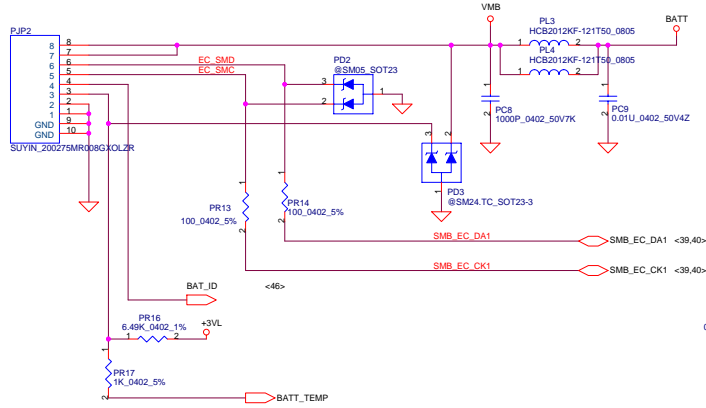
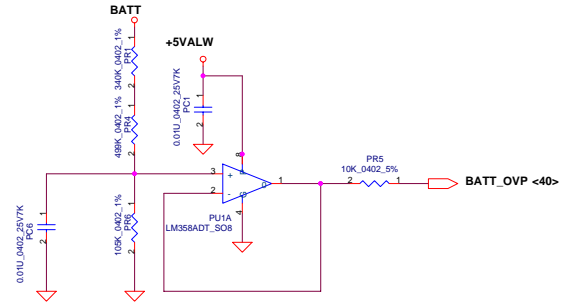
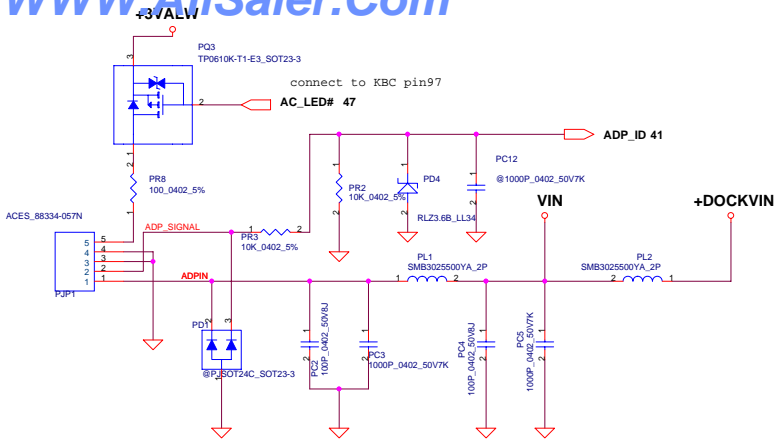
### Discharge circuit



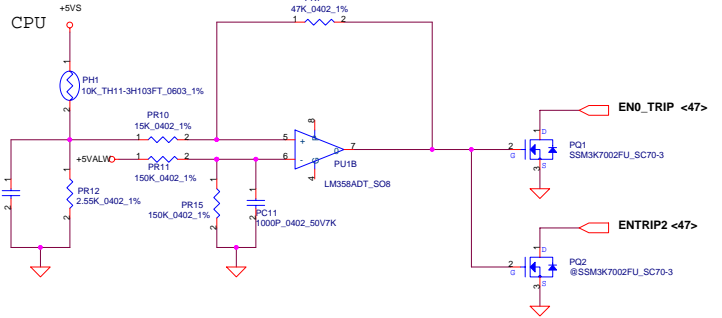
Security Classification		Compal Secret Data		Title	
Issued Date	2008/02/25	Deciphered Date	2008/02/25	DC/DC Interface	
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				Date	Monday, February 25, 2008
				Sheet	41 of 53



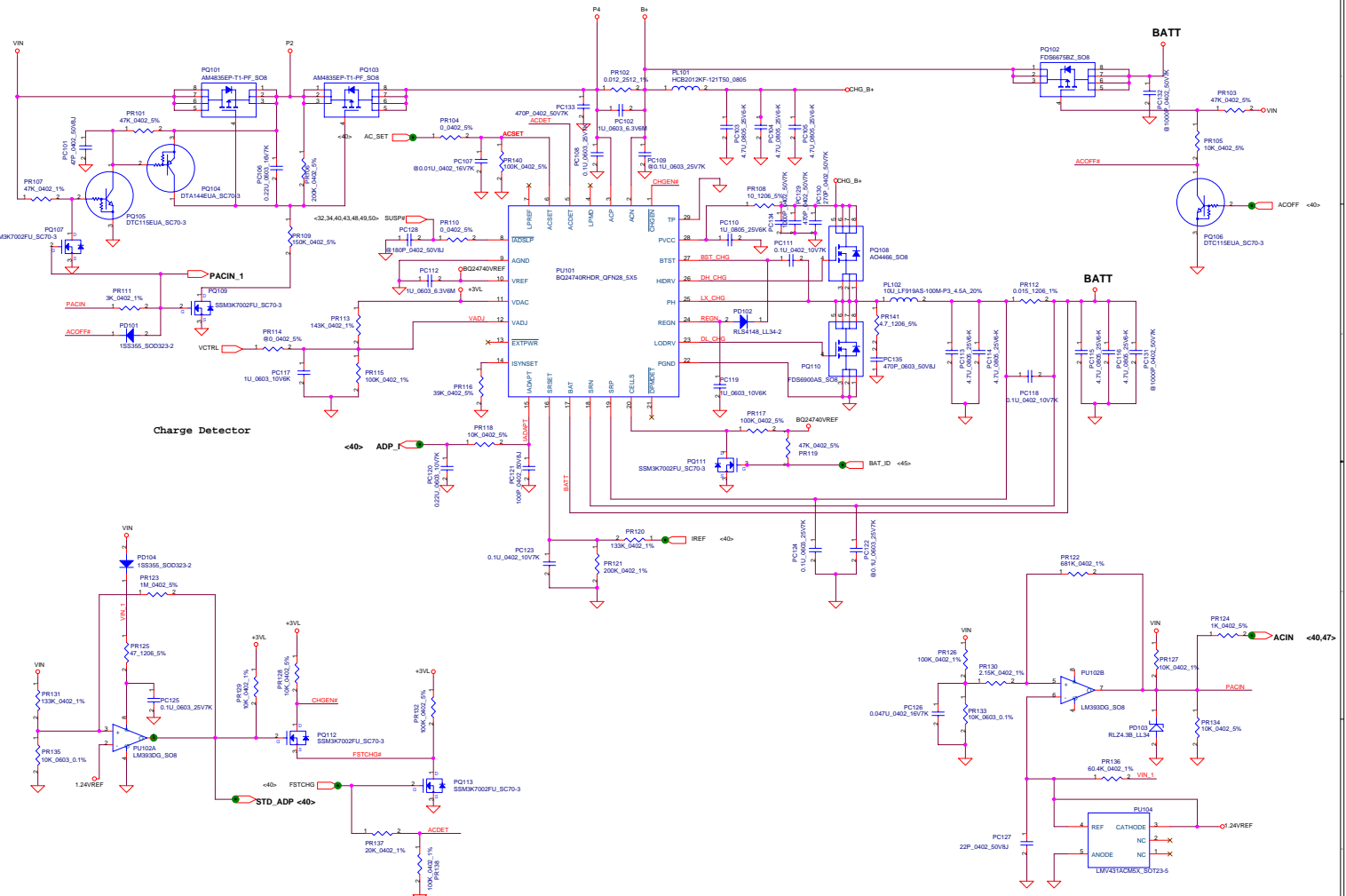
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/02/25	Deciphered Date	2008/02/25	Title
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				Custom
				LA-4102P Blade discrete
				Rev
				0.4
				Date
				Monday, February 25, 2008
				Sheet
				42 of 53



PH1 under CPU bottom side :  
CPU thermal protection at 90  $\pm$  3 degree C  
Recovery at 47  $\pm$  3 degree C

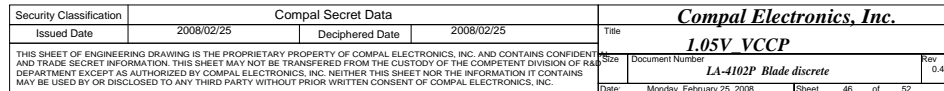


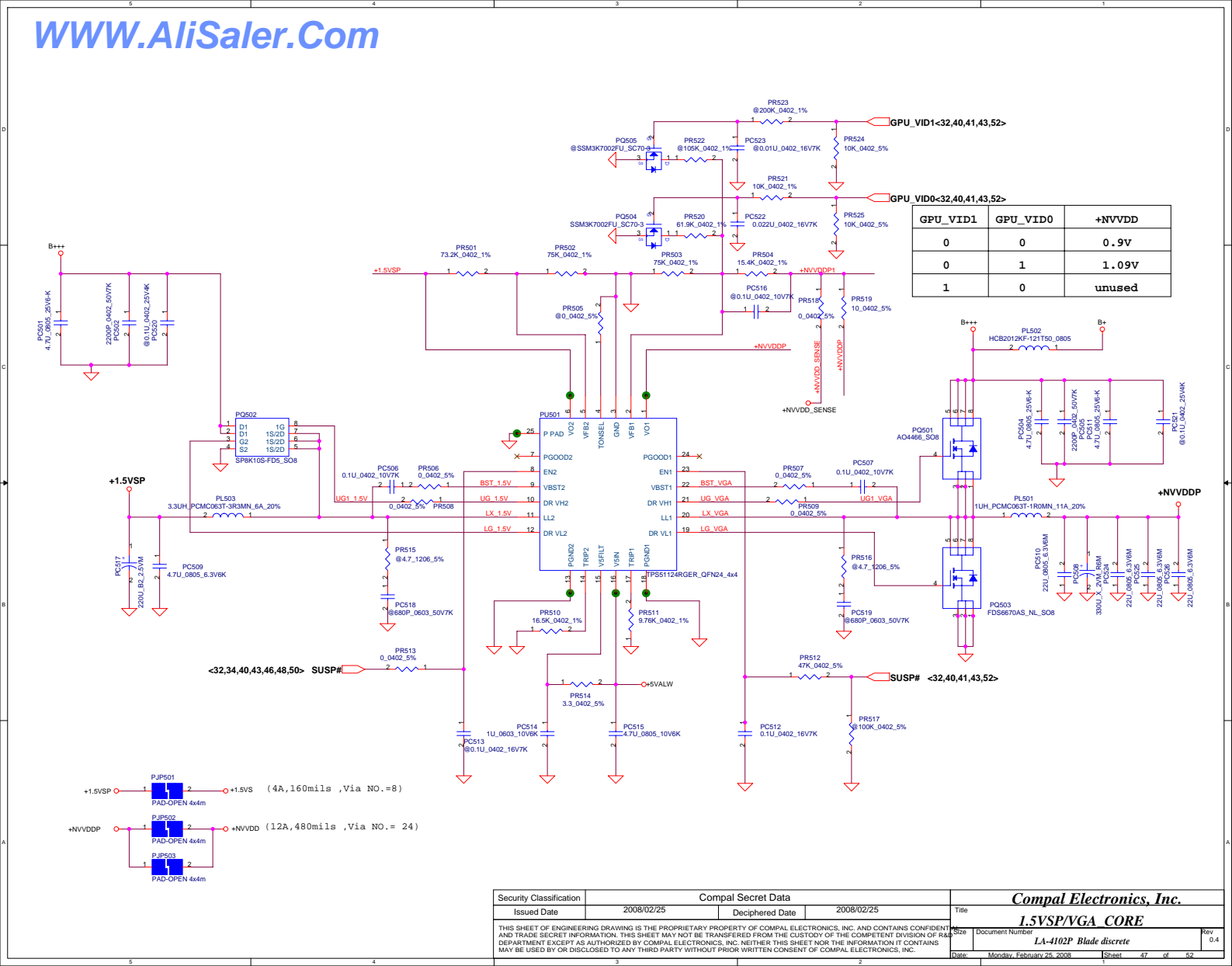
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008/02/25	Deciphered Date	2008/02/25	Title	DC Connector/CPU OTP
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Date: Monday, February 25, 2008					Sheet 43 of 52



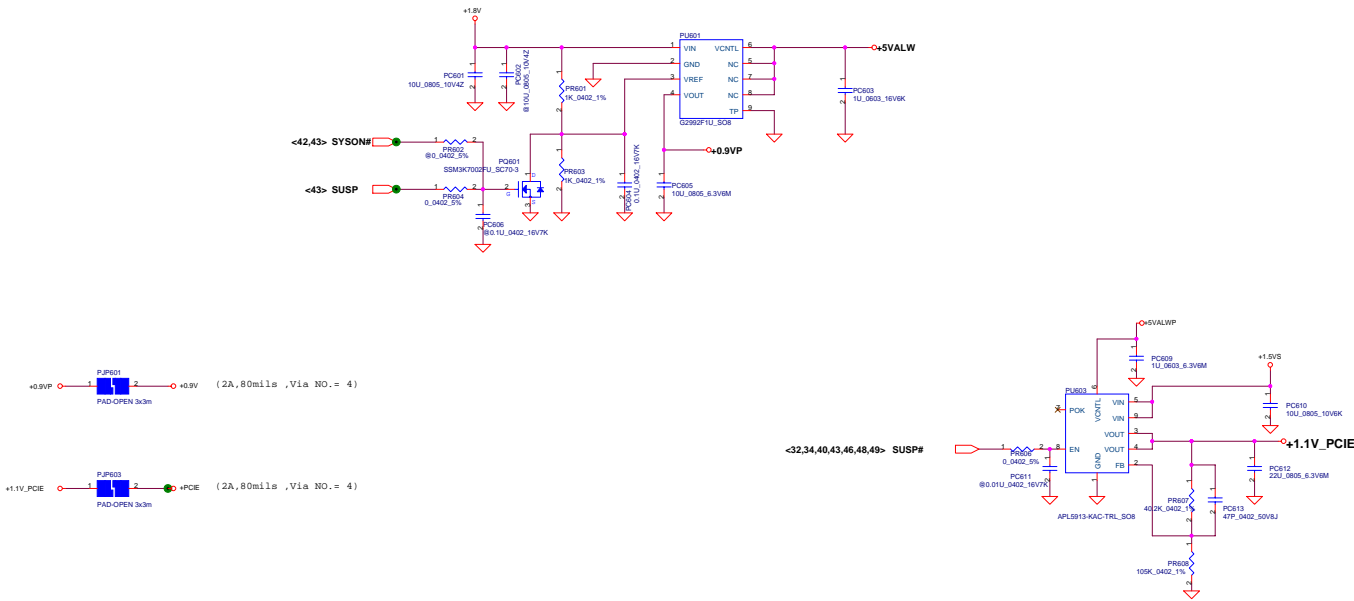
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Issued Date	2008/02/25	Deciphered Date	2008/02/25	Title	
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				Revision	0.4
				Drawn	0.4
				Checked	0.4
				Released	0.4





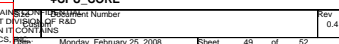


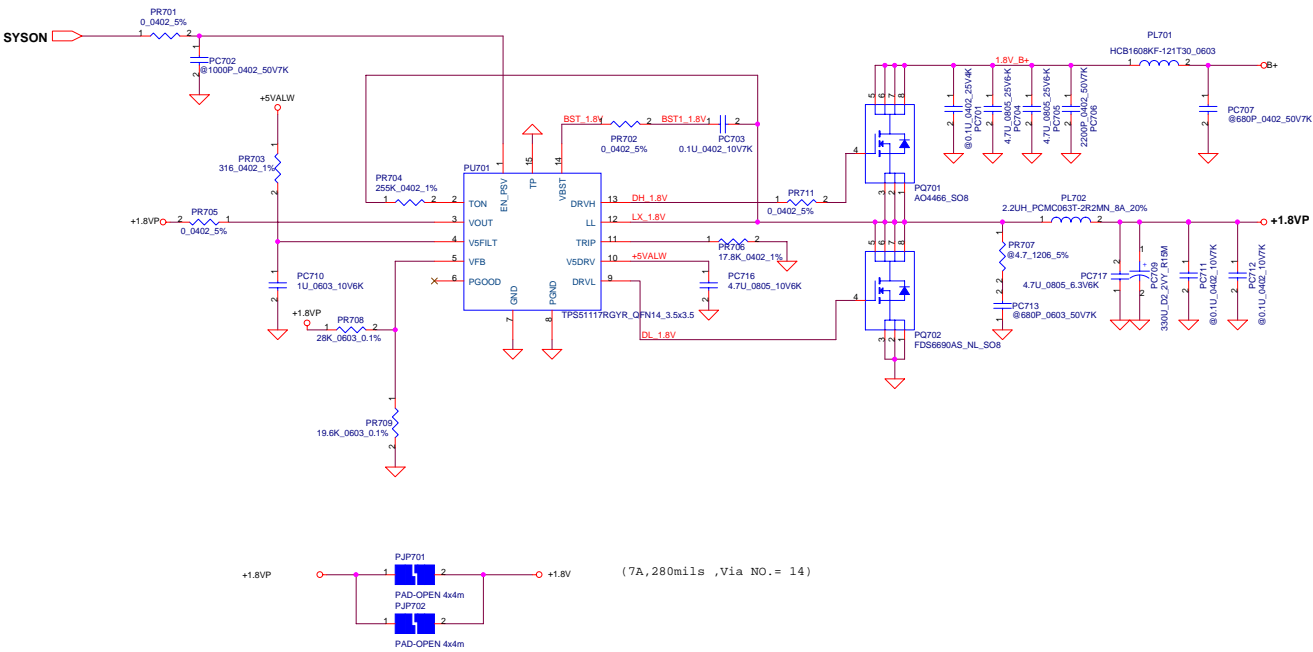
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LA-4102P Blade discrete				Monday, February 25, 2008
Sheet 47 of 52				



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				Document Number
				Rev
				Date
				Monday, February 25, 2008
				Sheet
				48
				51
				52
				53
				54







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				Document Number	LA-4102P Blade discrete
				Date	Monday, February 25, 2008
				Sheet	50 of 52
				Rev	0.4

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.																												
1	43	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12																													
2	45	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301, cancel PQ303.																													
3	44	Charger	11/06	Compal	EMI solution	Add PC128																													
4	49	CPU_CORE	11/06	Compal	EMI solution	Add PC240																													
5	47	1.5VSP/VGA_CORE	11/06	Compal	for VGA voltage steps	Add PQ505, PR523, PR524, PR525																													
6	45	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF																													
7	44	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133																													
8	49	+CPU_CORE	12/31	Compal	EMI solution	Add PC242																													
9	47	+1.5VSP/VGA COREP	01/02	Compal	HW request	Change PR513 to 0_ohm																													
10	44	Charger	01/02	Compal	EMI solution	Add PC135 and PR141																													
11	49	+CPU_CORE	02/15	Compal	Change high-side MOS for WWAN	Change PQ201 and PQ204 to powerpak																													
12	43	DC Connector /CPU_OTP	02/15	Compal	AC LED change to KBC control	ACLEd# connect to EC pin 97																													
13	43	DC Connector /CPU_OTP	02/19	Compal	WWAM issue	add PC241 47pF																													
14	49	+CPU_CORE	02/19	Compal	WWAM issue	add PC243 PC244 47pF																													
<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="3">Title</td></tr><tr><td>Issued Date</td><td>2008/02/25</td><td>Deciphered Date</td><td>2008/02/25</td><td>Size</td><td>Document Number</td><td>Rev.</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Custom</td><td>LA-4102P Blade discrete</td><td>0.4</td></tr><tr><td colspan="4"></td><td>Date</td><td>Monday, February 25, 2008</td><td>Sheet 51 of 52</td></tr></table>							Security Classification	Compal Secret Data			Title			Issued Date	2008/02/25	Deciphered Date	2008/02/25	Size	Document Number	Rev.	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Custom	LA-4102P Blade discrete	0.4					Date	Monday, February 25, 2008	Sheet 51 of 52	
Security Classification	Compal Secret Data			Title																															
Issued Date	2008/02/25	Deciphered Date	2008/02/25	Size	Document Number	Rev.																													
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				Date	Monday, February 25, 2008	Sheet 51 of 52																													

Item	Find Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41, C42, C43, C44 Change ESR=7m ohm	11/21	DB
2	Disable TV out function from Docking	20	TV signal unconnected,DACB_VDD pull low 10K (R948).	11/07	DB
3	Update Connetor Library		CRT(JCRT1), HDMI(JHDMI1), ESATA(JP53), Finger print(JP24), FAN(JP2), Speaker(JP60), Multi bay(JP12), Dual LED(D53, D54	11/17	DB
4	Delete LVDS B channel	19,20	Schematic Delete	11/17	DB
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K , R1093=100K,Add GPIO 20 to turn off power	11/07	DB
6	Reserve Card reader D3E function	27,32	GPIO6= CR_CPPE# , GPIO22=CR_WAKE#	11/17	DB
7	Swap PCIE LAN and New card	27	Swap PCIE4 and PICE6	11/17	DB
8	Change GPU 1.8VS power	20, 21	Change 1.8VS to +VDD_MEM18	11/17	DB
9	Change G sensor control from SB, LED drive by +5VS	27, 39	Change G sensor control from SB	11/17	DB
10	Avoid Battery mode can't boot issue	38, 45	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	DB
11	Add G sensor ST and Bosch	37	Add G sensor ST and Bosch	11/17	DB
12	Change LAN solution (Marvell to Realtek)	30	Change LAN solution (Marvell to Realtek)	11/17	DB
13	LAN transformer interfere	30	U19 Change to correct transformer type	11/17	DB
14	Cardreader schematic review,add D3E function	32	R709-->10K, R1047-->8.2K, R1128-->Stuff, R705-->@, U37-->@, Cardreader LED-->+5VS, add D3E function	11/17	DB
15	Jack can't detect normal	33	R1059 change from 39.2 to 39.2K	11/17	DB
16	Docking can not power on	40	Add power on circuit D57,Q13R751,R752,R753	11/17	DB
17	HP audio team recommend	33, 35	C1480-C1487, C1352, C1354 change to 0.022U, Amp output setup to 15.6 dB, Reserve C747, C748 for GNDA and GND	11/17	DB
18	Audio jack can't detect normal	35	Add Pull up resistor R750 to +3VALW	11/17	DB
19	Docking HP audio test fail	35	Add C795, C796 to avoid DC level, and add R968, R969 to reduce HP out level	11/17	DB
20	Leakage problem	38	Correct direction preteck leakage	11/07	DB
21	EC pin define update	38	Delete EC_PME#, SYSON PU, SUSP# PU, LID_SW# change to +3VALW, Delete CLKRUN#, R582->@ for C0 chip, C1R PU+5VL, add 100P to BATT_OVP(EC recommend)	11/07	DB
22	Can't Hibernation(SLP_S4#)	38	Connect SLP_S4# to SB	11/17	DB
23	EC can't receive docking present	40	CONA# change +3VL	11/12	DB
24	Reserve capacitor on digital MIC for EMI request	19	Add C496,C498	11/07	DB
25	Add 2N7002 to GND on HDMI to avoid leakage.	21	Add Q74	01/04	SI
26	+VDD_MEM18 to +1.8VS, change to jummpers	22	Delete R1124,R1125 add PJP605	01/04	SI
27	HDCP ROM fail. HDCP_SCL need pull high.	22	R224 no stuff. R213 stuff.	01/04	SI
28	Reserve capacitor on digital MIC for SED, WWAN noise	26	Add C499,C502	01/04	SI

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					LA-4102P Blade discrete
				Date	Monday, February 25, 2008
				Sheet	52 of 53
				Rev	0.4

Item	Find Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Change transformer vendor	30	change U19 library	01/04	SI
2	XMIT_OFF add a diode to avoid leakage.	31	Add D88	01/04	SI
3	Card reader recommend	32	XD_ALE need pull +3VS not pull low.	01/04	SI
4	change Q54 from transistor to MOS for cardreader LED.	32	Change Q54	01/04	SI
5	speaker pop issue	35	Change C1488 to 1U	01/04	SI
6	Reserve capacitor on SPL_FSEL#,CLK#,FER for EMI request	36	Add C2125,C2126,C2127	01/04	SI
7	Change EC_PME pull high from +3VL to +3VALW	38	R585 stuff	01/04	SI
8	Reserve damping resistor on SPL_CLK for EMI request	38	Add R191	01/04	SI
9	WLAN LED issue,WL_BLUE_LED# pull +3VS	39	Add R716	01/04	SI
10	Add bypass capacitance on sensor bottom	39	Add C261(4.7U)	01/04	SI
11	EC can't detect DOCK_PRESENT.	40	change R754 to 22 Ohm,R623 to 2K	01/04	SI
12	Add DOCK_VOL_UP#,DOCK_VOL_Down# pull +3VS	40	Add R594,R596	01/04	SI
13	SPDIF issue	40	follow Vader	01/04	SI
14	Docking CRT blurred	40	Change ping 31,39,22 connect to GND	01/04	SI
15	Change R650 and C770 to modify the power sequence	41	change R650 to 1K, C770 to 0.1u	01/04	SI
16	Add 12P on CLK_14M_ICh for WWAN noise	17	Add 12P on CLK_14M_ICh	02/15	PV
17	BKOFF# reserve pull low 10K	19	reserve R717	02/15	PV
18	Reserve CMD27 to support 64M X16	7,8	Reserve CMD27 to support 64M X16	02/15	PV
19	Reserve cap on HDA_BITCLK for WWAN noise issue	26	Reserve cap on HDA_BITCLK	02/15	PV
20	Reserve to prevent ESD issue	30	Reserve ESD diode on LAN LED pin	02/15	PV
21	Change WLAN and WWAN 0402 resistor to 0805	31	Change WLAN and WWAN 0402 resistor to 0805, and WLAN change to +3VS power plane	02/15	PV
22	Direct drive LED, and add D3E function diode	32	Direct drive LED and XD_ALE Pull L, and add D86 for D3E function	02/15	PV
23	Change R1092 value on BT power switch Gate	36	Change R1092 to 10K	02/15	PV
24	Correct AC_LED control by EC	38	AC_LED Change controll by EC	02/15	PV
25	Change all LED limit current resistor to 200 ohm	39	Change all LED limit current resistor to 200 ohm and add Touch pad LED for PR	02/15	PV
26	Add 33 ohm for MUTE_LED and DOCK_SLP_BTN#	40	Add 33 ohm for MUTE_LED and DOCK_SLP_BTN#	02/15	PV
27	follow check list ver:1.5	6	change R13 to 56 ohm;change R2~R8 to 51 ohm;change R11 to 0ohm	02/20	PV
28	Reserve Cap for EMI	42	add C1250,C1249	02/20	PV

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					LA-4102P Blade discrete
				Date	Monday, February 25, 2008
				Sheet	53 of 53
				Rev	0.4

Item		Revised Issue (Reason for change)	PAGE	Modify List	Date	Phase
1		follow check list Ver:1.5	17	reserve R148	02/15	PV
2		follow check list Ver:1.5	9	change R45,R48 to 10K	02/15	PV
3		boot code "88" power sequence fail	27	add Diode from PWROK to RSMRST	02/15	PV
4		Change BT,LAN,DOCK,Multibay connect for DFX			02/15	PV
5		Change WWAN and WLAN LED	39		02/15	PV
6		For EMI	37	SPL_CLK add R2118 , R2119 , R2120 => 33ohm add C2125 , C2126 , C2127 => 22pF;R553, 554, 556 =>10ohm	02/15	PV
7		For EMI	30	LAN add C656 and C657 => 0.1uF	02/15	PV
8		For EMI	39	T/P add D28 and C729	02/15	PV
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				Sheet	54 of 53
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